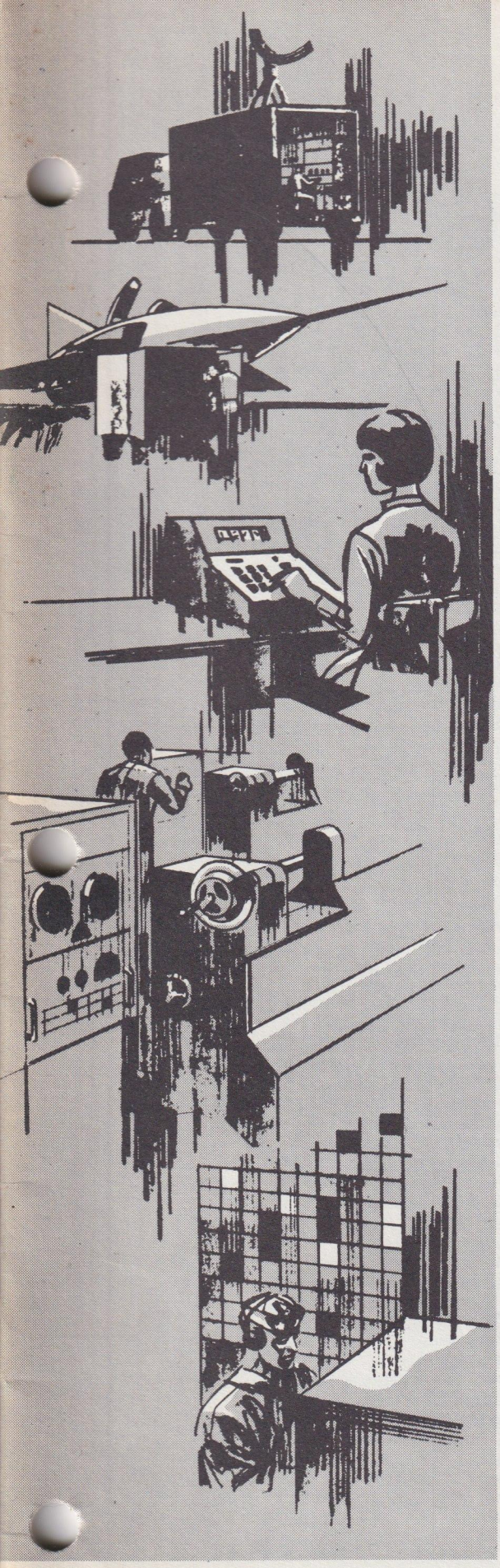

Charles E Perkett

SIGNETICS

JANUARY 1967

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UTILOGIC

APPLICATIONS HANDBOOK

SIGNETICS CORPORATION • 811 EAST ARQUES AVENUE, SUNNYVALE CALIFORNIA • TEL: (408) 739-7700 • TWX: (910) 339-9220

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INTRODUCTION

The UTILOGIC family of digital integrated circuits is designed specifically for application in military ground support and commercial/industrial equipment. This book presents the systems designer with a broader view of the UTILOGIC family characteristics, their application rules and examples than possible in data sheets.

UTILOGIC elements are available in two temperature ranges; those with SU prefixes are for applications in the -20°C to +85°C range, and those with LU prefixes in the +10°C to +55°C range. The SU elements are available in either Signetics "G" package, a 10-lead glass-kovar flat package (JEDEC TO-91) or a Signetics "K" package, 10-lead low-profile "can" (JEDEC TO-100). The LU elements are available in "K" packages only. Both the low and the high temperature series contain the following elements:

Dual 3-Input Gate Expander (LU/SU300)
Single 6-Input AND Gate (LU/SU305)
Dual 3-Input AND Gate (LU/SU306)
Single 7-Input NOR Gate (LU/SU314)
Dual 3-Input NOR Gate (LU/SU315)
Dual 2-Input Expandable NOR Gate (LU/SU316)
J-K Binary Element (LU/SU320)
Dual 2-Input Expandable OR Gate (LU/SU331)
Dual 3-Input OR Gate (LU/SU332)

UTILOGIC CIRCUITS

UTILOGIC inputs are classified as sink loads and source loads by the direction of current flow required to activate the input. The input of the OR and NOR gates and the preset (P_j, P_k) inputs of the Binary are called source loads because they must be driven by a source of current, e.g., the output of a UTILOGIC element in the "1" state or a connection to the positive supply. The inputs of the AND gates and the synchronous (J, K, C) inputs of the Binary are called sink loads because they must be driven from a current sink; for example, the output of a UTILOGIC element in the "0" state or a connection to ground.

In this publication, and all other UTILOGIC literature, the convention of positive logic, i.e., the positive level is "1", has been assumed. If the negative logic notation is assumed (most negative level is "1"), the AND, OR, and NOR gates become OR, AND, and NAND respectively.

The characteristic curves presented in the various sections are designed to allow the system designer to predict system performance characteristics for various operating conditions. In general, characteristics are normalized to the conditions of the specification sheets. The use of the normalized characterisitic is a definite design aid in that it is usually the change in the characteristic as a result of a change in the parameter that is of interest. As long as the effects, e.g., $\frac{\partial Vsat}{\partial Temp.}$, are small, the total effect may be predicted by taking the product of the individual effects.

Throughout the discussion that follows, V_{cc} is assumed to be +4.5V unless otherwise specified.

AND Gates

The UTILOGIC AND gates (SU305, SU306, LU305, LU306) are fabricated from the same basic chip, and therefore have identical electrical characteristics. The internal connection pattern is varied to produce a single 6-input AND gate in the 305, and the dual 3-input AND gates in the 306.

CIRCUIT DESCRIPTION

Schematic diagrams of the UTILOGIC AND gates are shown in Figures 1 and 2. The multiple-emitter input structure provides the same function

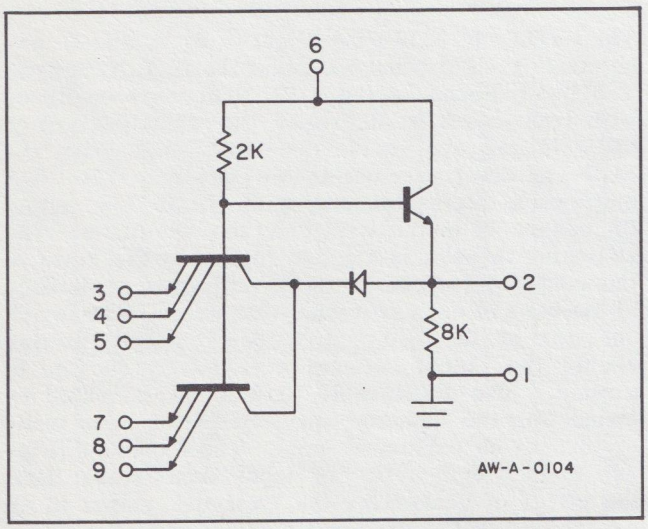


Figure 1 305 6-Input AND Gate

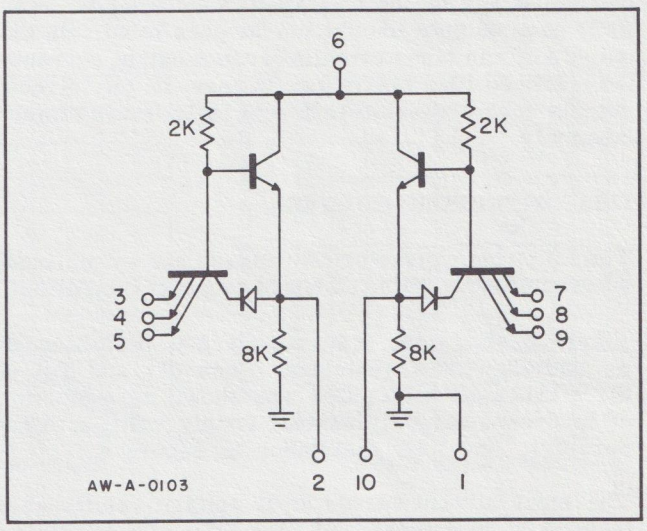


Figure 2 306 Dual 3-Input AND Gate

as a Diode AND gate. The output-emitter follower provides the current gain necessary for high fan-out, and also reduces the offset voltage associated with Diode AND gates. The emitter follower provides a low output impedance to effect fast response on "0" to "1" transitions and the current gain necessary for source current fan-out. The input transistor and connecting diode provide a low impedance circuit to maintain good response on "1" to "0" transitions. The output resistor ensures low steady-state "0" voltages.

INPUT CHARACTERISTICS

The input of the AND is defined as the standard UTILOGIC Sink Load. The maximum current from a Standard Sink Load is -2.1mA. A Standard Sink Load may be simulated by a 2KΩ resistor with series diode to the supply voltage. Input capacitance is 5 pf maximum, but typically will be 2.5 pf. The input impedance of UTILOGIC AND Gates is low enough so that unused inputs may be left open without degrading circuit performance. (Open inputs are logical "1".) However, unused inputs may be connected to used inputs of the same circuit without increasing the DC loading. The effect of the added capacitance is generally negligible.

OUTPUT CHARACTERISTICS

The AND gates will supply a current of -2mA at a minimum output level of 3.15 volts with a 3.3 V at the inputs. Fan-out is 10 to Standard UTILOGIC Source Loads. The AND gate does not have output current sinking capability; therefore, it cannot drive sink loads. Offset voltage is the difference between input and output voltage levels; for "1" inputs of 3.3 volts, the maximum offset is 0.15 volts (output lower than input) with a -2mA output current; for "0" input levels of 0.6 volts, the maximum offset -0.3 volts (output higher than input). The AND gate can drive any of the UTILOGIC source loads. The AND gate outputs should not be paralleled with the outputs of any other circuits because output currents may exceed the maximum ratings if the circuit outputs try to assume different logic levels simultaneously.

CHARACTERISTIC CURVES

The following characteristic curves are normalized, when applicable, to the standard data sheet conditions.

Figure 3 shows the test circuit and definition of T_1 and T_2. The switching times (T_1 and T_2) of the UTILOGIC AND gates are shown as a function of load capacitance, fan-out, supply voltage, temperature, and load resistance in Figure 4.

The input current versus input voltage relationship is vital at interfaces and also allows computation of margins at non-standard conditions of fan-out. Offset voltage, which is defined as the input voltage minus the output voltage, is shown in Figure 5 as a function of temperature. Full rated load current is applied to the outputs. Input voltages correspond to worst case UTILOGIC or Binary Element "1" and "0" output voltage levels.

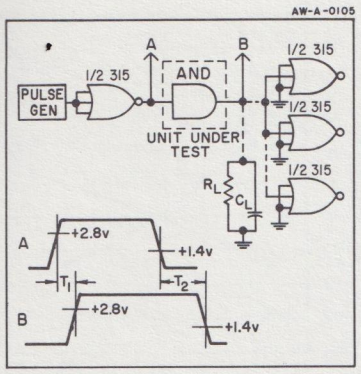
UTILOGIC NOR Gates and EXPANDER

The UTILOGIC NOR gates (SU314, SU315, LU314, and LU315), Expandable NOR gates (SU316 and LU316), and Expandable (SU300 and LU300), are all derived from the same basic circuit die to ensure full compatibility of the Expandable Gates and Expander, and to give all the circuits identical electrical characteristics. However, the 300 and 316 will have longer turn-off delay times (T_2) because of the additional capacitive loading on the expansion input. Turn-on delays (T_1) are not sensitive to this capacitance because the source impedance is low during turn-on.

The 300 Expander circuit is characterized in terms of its operation in conjunction with the 316 Expandable NOR and 331 Expandable OR. The ways in which 300 and 316 (and 300 and 331) compatibility are guaranteed are of interest. The Expansion Forward Voltage for the 300 and the Expansion Input Voltage of the 316 are measured under the same conditions, and the same limits are guaranteed. In addition, the 300 Input Leakage Current and the 316 "0" Input Current specifications guarantee reverse current compatibility. These specifications assure the user that the 300 and 316 or the 300 and 331 combination will have the same DC characteristics as when the 316 or 331 is used alone. AC characteristics are shown later (with the 316 and 331 curves) as a function of the capacitance on the Expansion Input.

CIRCUIT DESCRIPTION

The UTILOGIC NOR gate (Figures 6, 7, and 8) may be considered as a derivation of the DTL NOR gate. The input diodes of the DTL NOR were replaced with transistors to decrease the input current to allow larger source fan-out capabilities from the NOR and other circuits in the family. The NOR employs a totem-pole output to obtain low output impedance in both the "1" and the "0" states. The switching thresholds are determined by the ratio of the coupling resistance to the pull-down resistance at the base of each switching transistor. The series resistor at the output provides current-limiting should the output become accidentally shorted to ground. The Expandable NOR is implemented by connecting the common emitters of the input transistors to an expansion input. The Expander (Figure 9) is a dual array of input transistors; thus, the effect of connecting the Expander output to an expansion input is the same as connecting more input transistors in parallel.



TEST CIRCUIT AND WAVEFORMS

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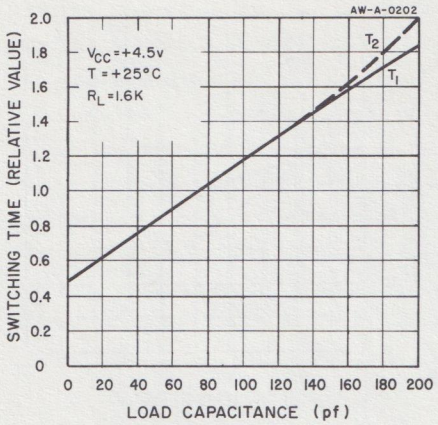

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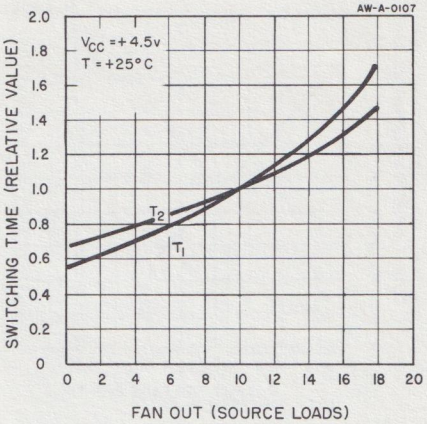

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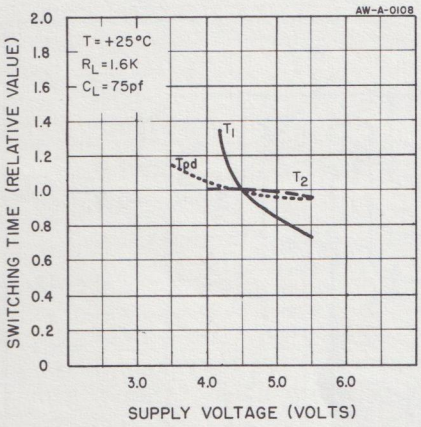

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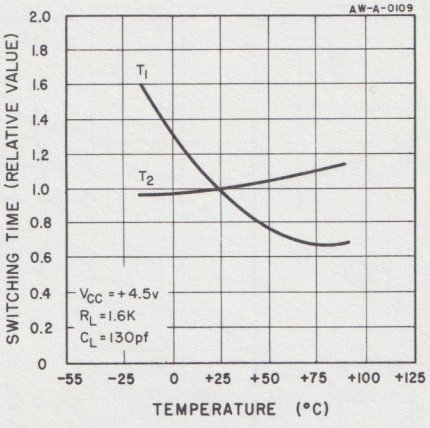

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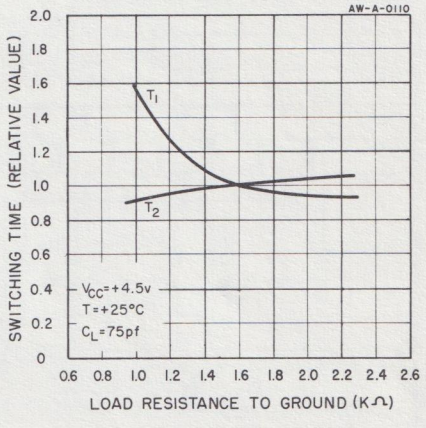

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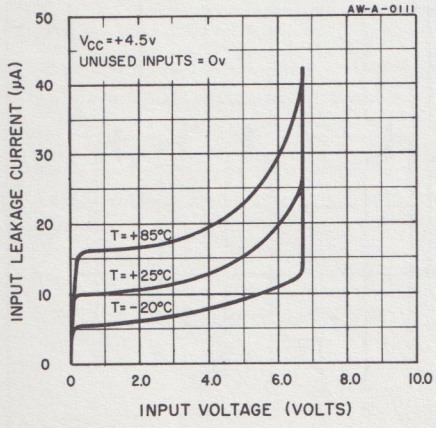
Figure 3 AND Gate Switching Characteristics



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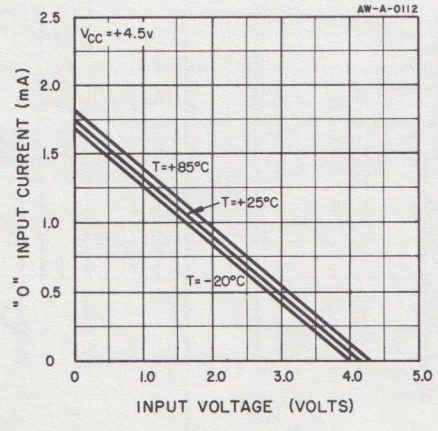

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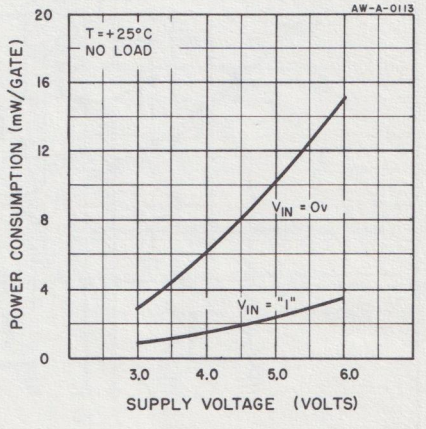

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Figure 4 AND Gate DC Characteristics

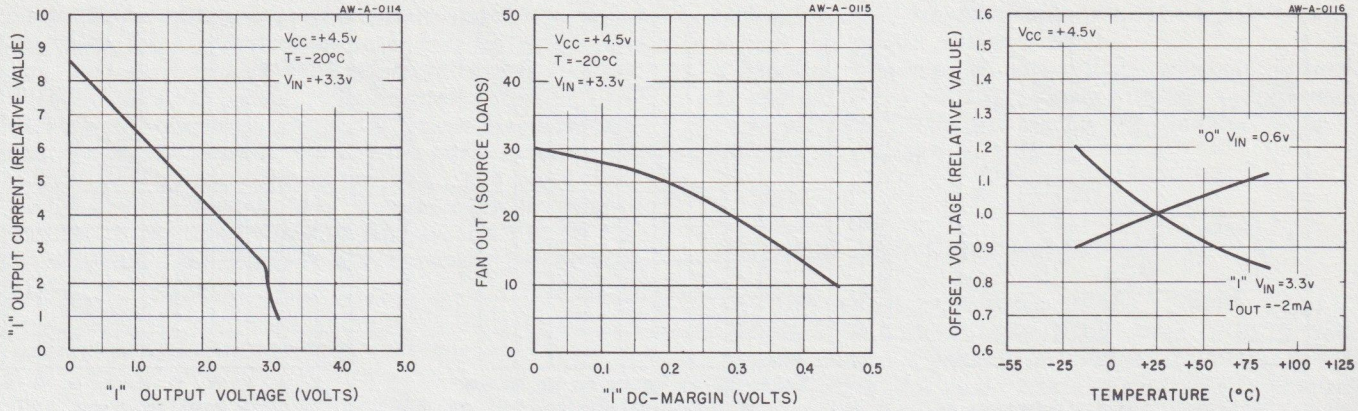

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Figure 5 AND Gate DC Characteristics

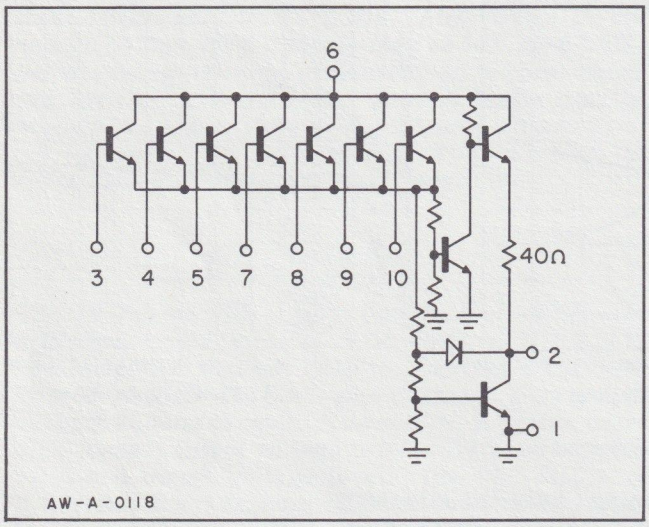


Figure 6 314 7-Input NOR Gate

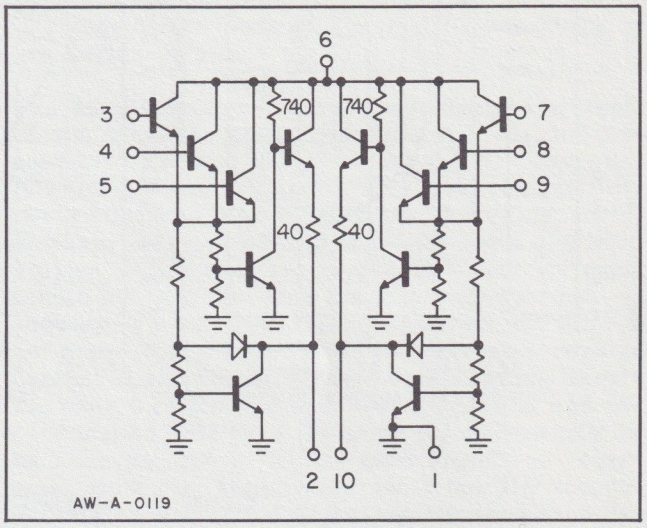


Figure 7 315 Dual 3-Input NOR Gate

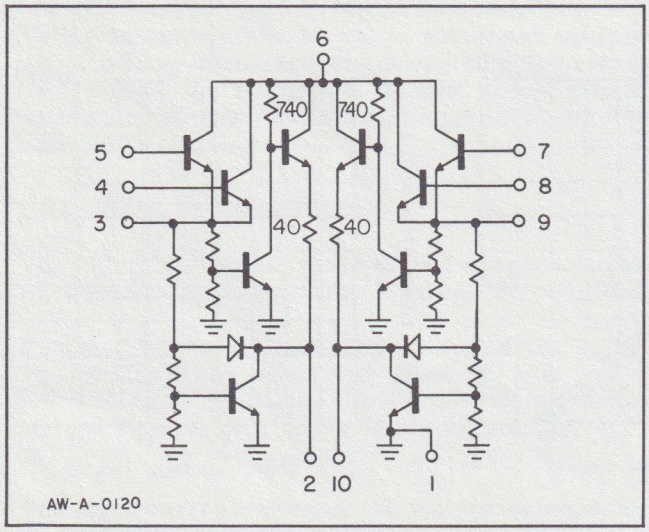


Figure 8 316 Dual 2-Input Expandable NOR Gate

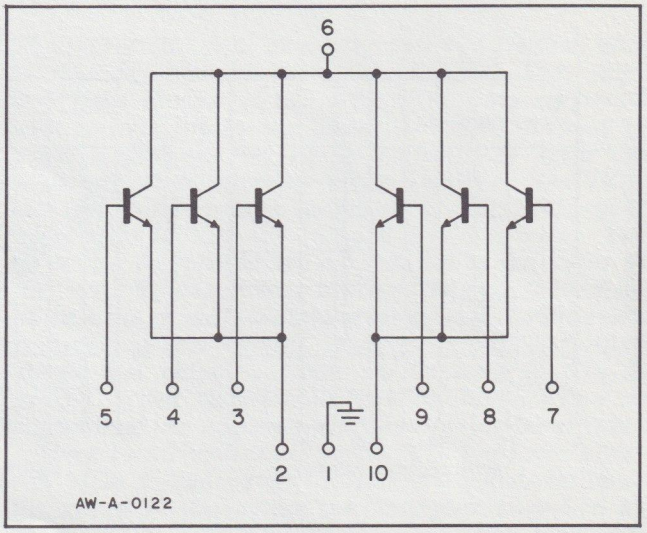
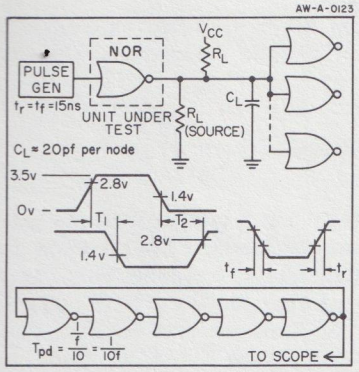


Figure 9 300 Dual 2-Input EXPANDER



TEST CIRCUITS AND WAVEFORMS

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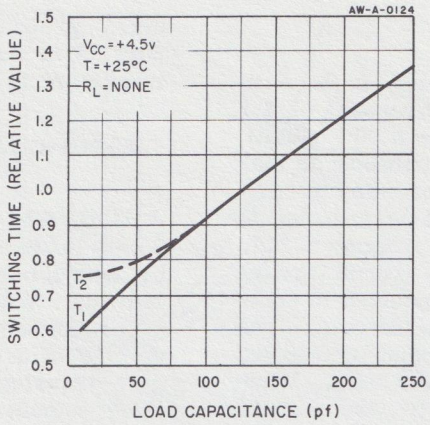

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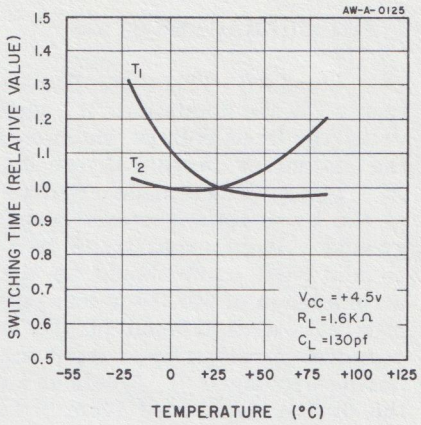

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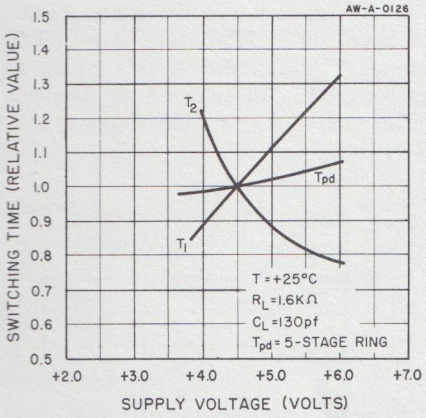

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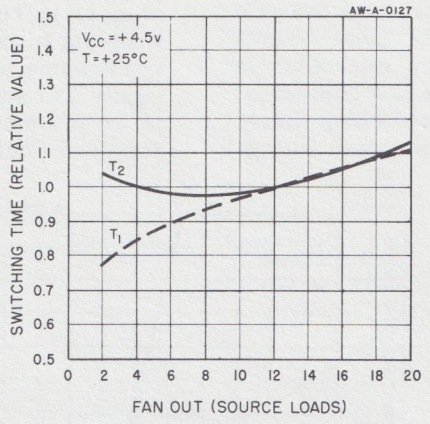

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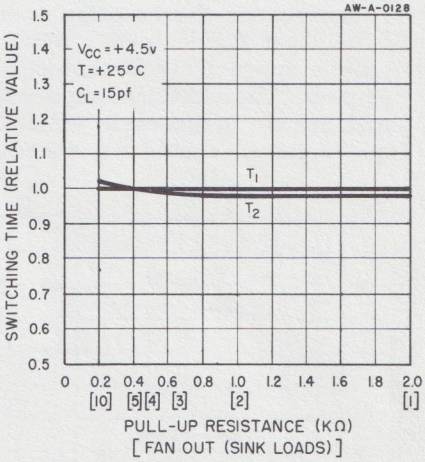

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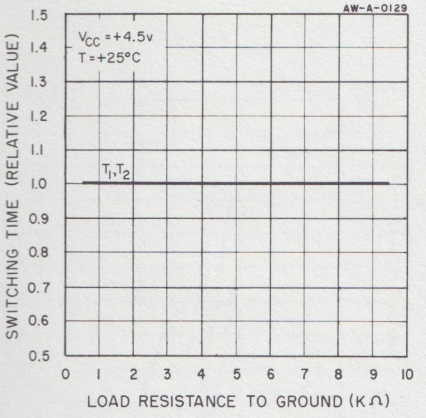

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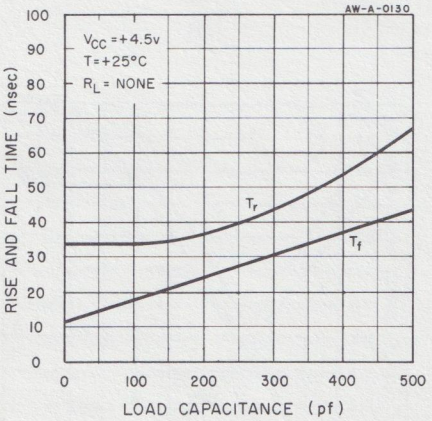

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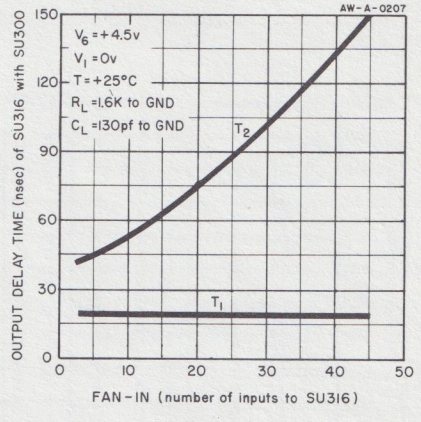


I

Figure 10 NOR Gate Switching Characteristics

INPUT CHARACTERISTICS

The Standard UTILOGIC Source Load is the NOR input. At the maximum "1" input threshold of 2.7 volts (the input voltage which ensures a "0" output), the maximum current drawn by a unit source load is 0.14mA. The Standard Source Load may be simulated by a 10KΩ resistor and 2 series diodes to ground. Input capacitance is 5 pf maximum. An unused NOR input should be tied to ground through a resistance of 60KΩ (or less) or connected in common with a used input on the same circuit. The capacitance of an open input may become charged during prolonged "1" levels at a driven input. When the driven input goes from "1" to "0", the charged capacitance discharges into the input and gives the effect of a slow circuit. Two or more common inputs represent the same DC load as a single input since the "1" input current is determined by the voltage across the coupling resistors and the gain of the input transistors. Neither of these values changes appreciably when inputs are connected in common. The additional capacitance of a commoned input has no measurable effect on switching times. Input voltages should not exceed the supply voltage unless precautions are taken to limit the resulting current in the collector-base junction of the input transistor to 30mA.

OUTPUT CHARACTERISTICS

A UTILOGIC NOR gate has a guaranteed fan-out of 5 sink loads and 12 source loads. All 17 loads may be connected simultaneously because they do not interact. When driving sink loads, a NOR gate has a current capability of 2mA at a minimum output voltage of 3.3 volts. Because the NOR gates employ transistors for both pull-up and pull-down, their outputs cannot be connected in parallel with the output of any other independent circuit. Parallel operation of an active device with another device may result in ambiguous output voltages and/or excessively high currents if one device should attempt to reach a "1" level while the other is attempting to reach a level "0". However, two NORS in the same package may be connected with common inputs and common outputs. In this case, fan-out is 34 (24 source plus 10 sink) and the input is two Standard Source Loads.

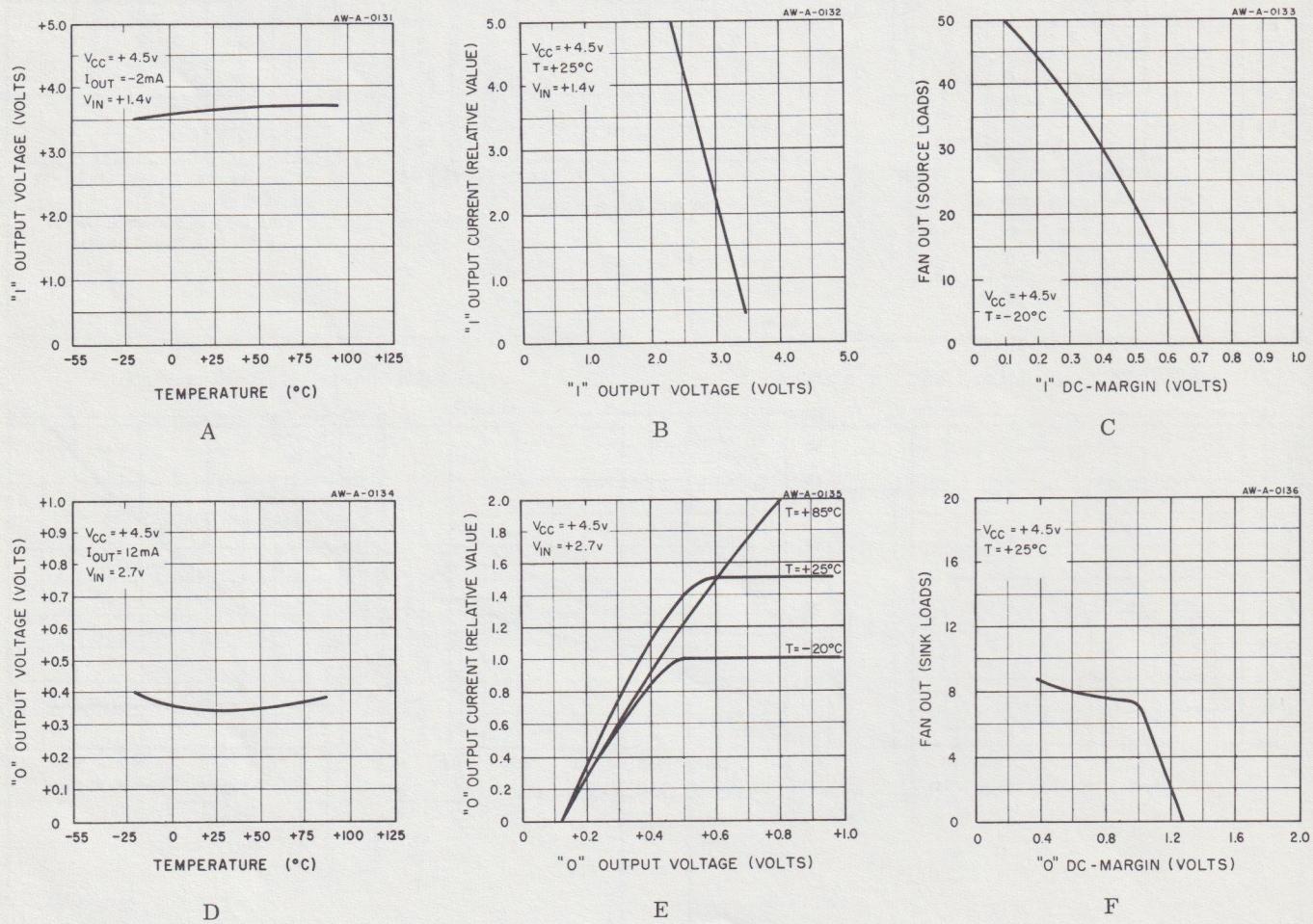
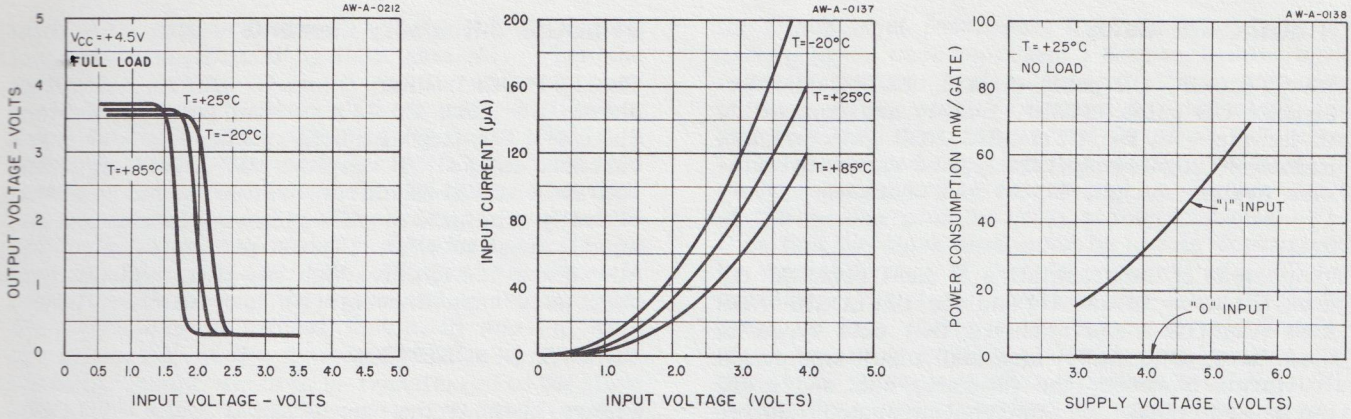
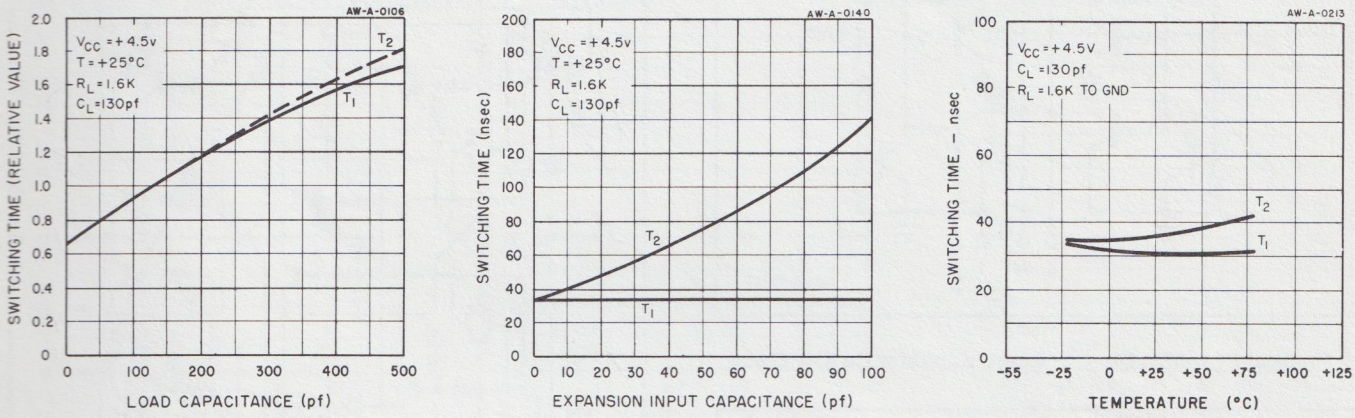


Figure 11 NOR Gate DC Characteristics



A B C

Figure 12 NOR Gate DC Characteristics



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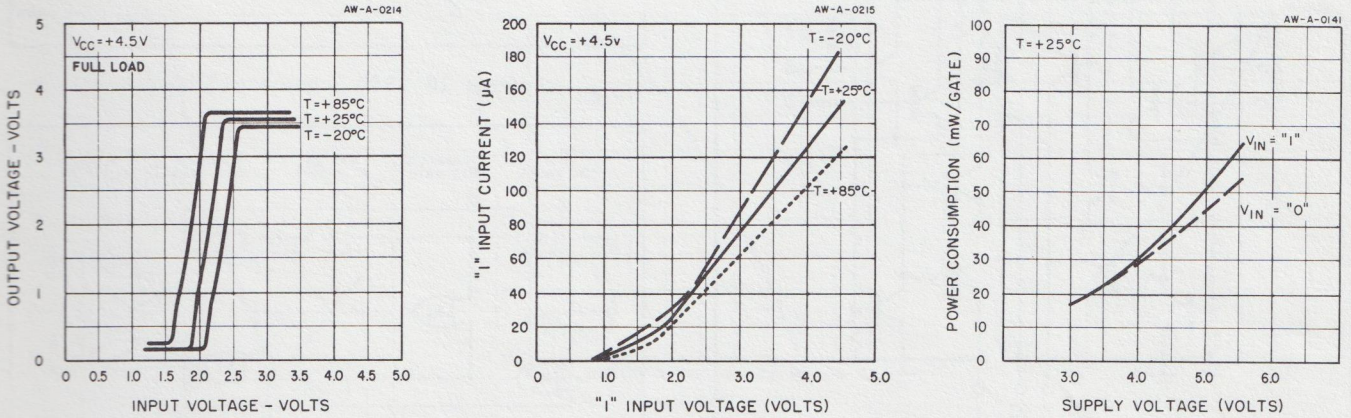


D E F

Figure 13 OR Gate Characteristics

UTILOGIC OR Gates

The UTILOGIC OR gates (SU332, LU332) and Expandable OR gates (SU331, LU331) are compatible pin-for-pin with the UTILOGIC NOR gate and Expandable NOR gate respectively, and therefore simplifies system design, layout and checkout.

Comparison of the schematics of the UTILOGIC OR gates (Figures 14 and 15) and the UITLOGIC NOR gates (Figures 7 and 8) shows that both types of gates have essentially identical input and output structures; however, the OR gates use one more transistor to obtain the additional inversion required to produce an OR gate from the basic UTILOGIC NOR configuration.

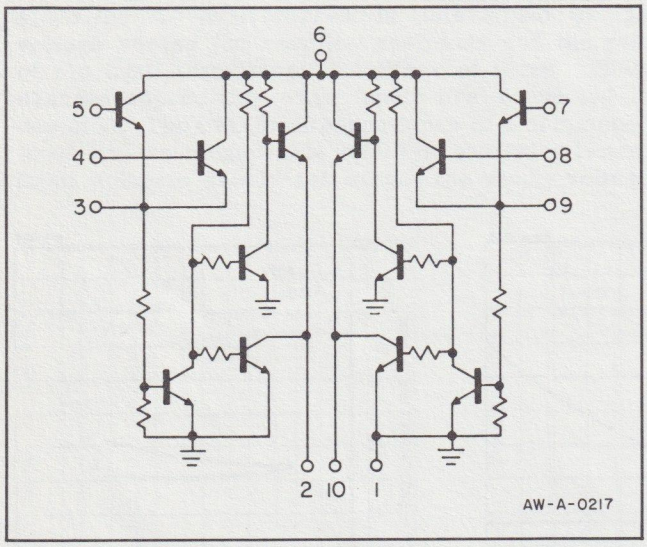


Figure 14 331 Dual 2-Input Expandable OR Gate

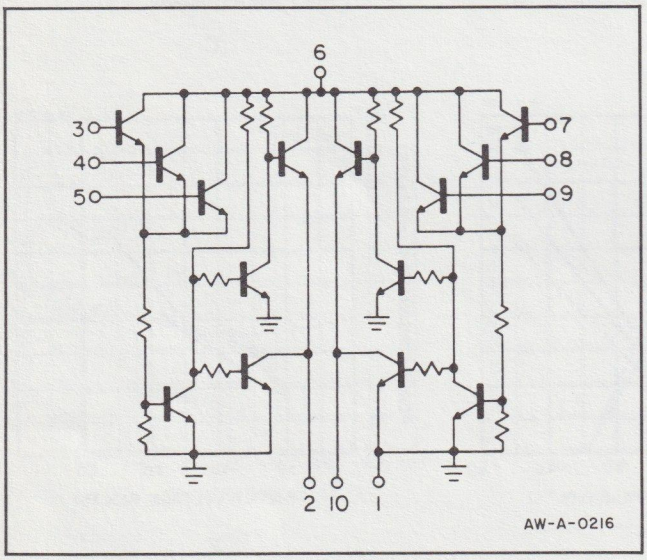


Figure 15 332 Dual 3-Input OR Gate

UTILOGIC J-K Binary Elements

The UTILOGIC Binary Element (SU320, LU320) as shown in Figure 16, is a general purpose Master-Slave J-K flip-flop with both synchronous and asynchronous inputs. It employs DC-level triggering and internal-threshold separation techniques that virtually eliminate clock-waveform restrictions and signal race problems. Totem-pole output circuitry allows the 320 to drive high fan-outs (and the high associated capacitances) with low switching times.

CIRCUIT DESCRIPTION

Figure 17 shows the functional parts of a UTILOGIC Binary Element that are derived from Diode AND gates and modified UTILOGIC NOR gates. NORS N1 and N2 form a latch-type master flip-flop; NORS N4 and N5 form the slave flip-flop. The input AND gates, A1 and A2, control the entry of information into the master. The transfer AND gates, A3 and A4, control the transfer of information from the master to the slave and are disabled whenever either

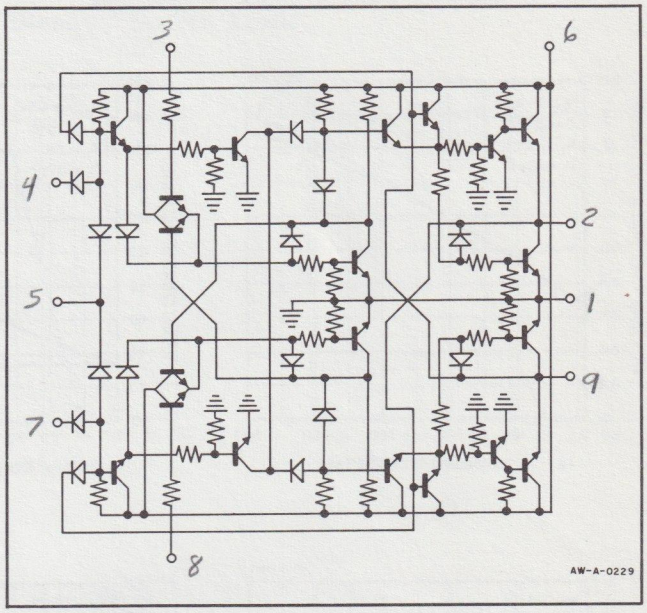


Figure 16 320 Schematic Diagram

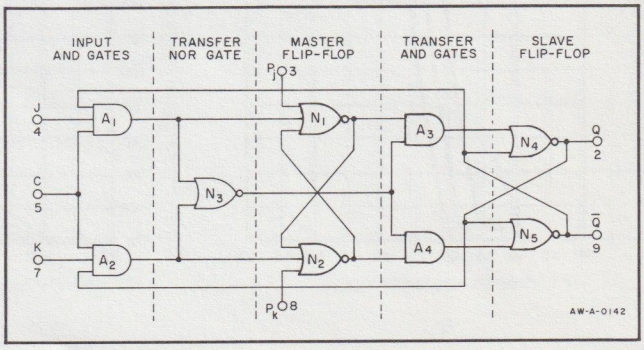


Figure 17 320 Logic Diagram

input AND gate is enabled. The clock-separating function is performed by NOR gate N3. When the clock line is low, N3 is off and the slave is connected to the master through the transfer AND gates. A rising clock pulse will turn N3 on at about 1.1 volts to disable the transfer AND gates and will reach the switching thresholds of the master flip-flop at about 2.2 volts to allow entry of input information. When the clock pulse falls to the 1.1 volts level, the transfer AND gate will allow the new state to be transferred to the slave and to the outputs. The asynchronous (preset) inputs, P_j and P_k, have direct control of the master flip-flop.

To allow preset states to be transferred to the slave and to the outputs, the transfer AND gates must be enabled by lowering the clock line or the J-K inputs. One of the input AND gates always is disabled by the feedback loops from the outputs; therefore, it is only necessary to lower J when presetting Q to "1" and K when presetting Q to "0". Simultaneous "1" levels at both the P_j and P_k inputs will cause the outputs of both N1 and N2 to be low, therefore, no information transfer may occur and the state of the Binary will not be changed.

INPUT AND OUTPUT CHARACTERISTICS

The J and K inputs each represent 0.5 Sink Load; the Clock input represents 0.75 Sink Load; the P_j and P_k inputs each represent 1 Source Load. Input capacitances are 5 pf maximum. The worst-case positive pulse widths required for the clock and preset inputs are 110 ns and 80 ns at 2.7 volts. In a DC-clocked flip-flop like the 320, the positive clock requirement is determined by the latch time of the master plus the delay of the input gate. The time that the clock input must be low is determined by the latch time of the slave (specified as T_2 for the 320). The logic levels at the J and K inputs must be at a stable state before the clock pulse rises and must remain stable during the time that the clock pulse is high. Allowing J or K to fall before the clock pulse has the same effect as narrowing the clock pulse.

J	K	Q	P_j	P_k	Q
0	0	Q	0	0	Q
0	1	0	0	1	0
1	0	1	1	0	1
1	1	$\overline{Q}$	1	1	*
Synchronous inputs at clock time			Asynchronous inputs *See text on presetting		

Figure 18 320 Truth Table

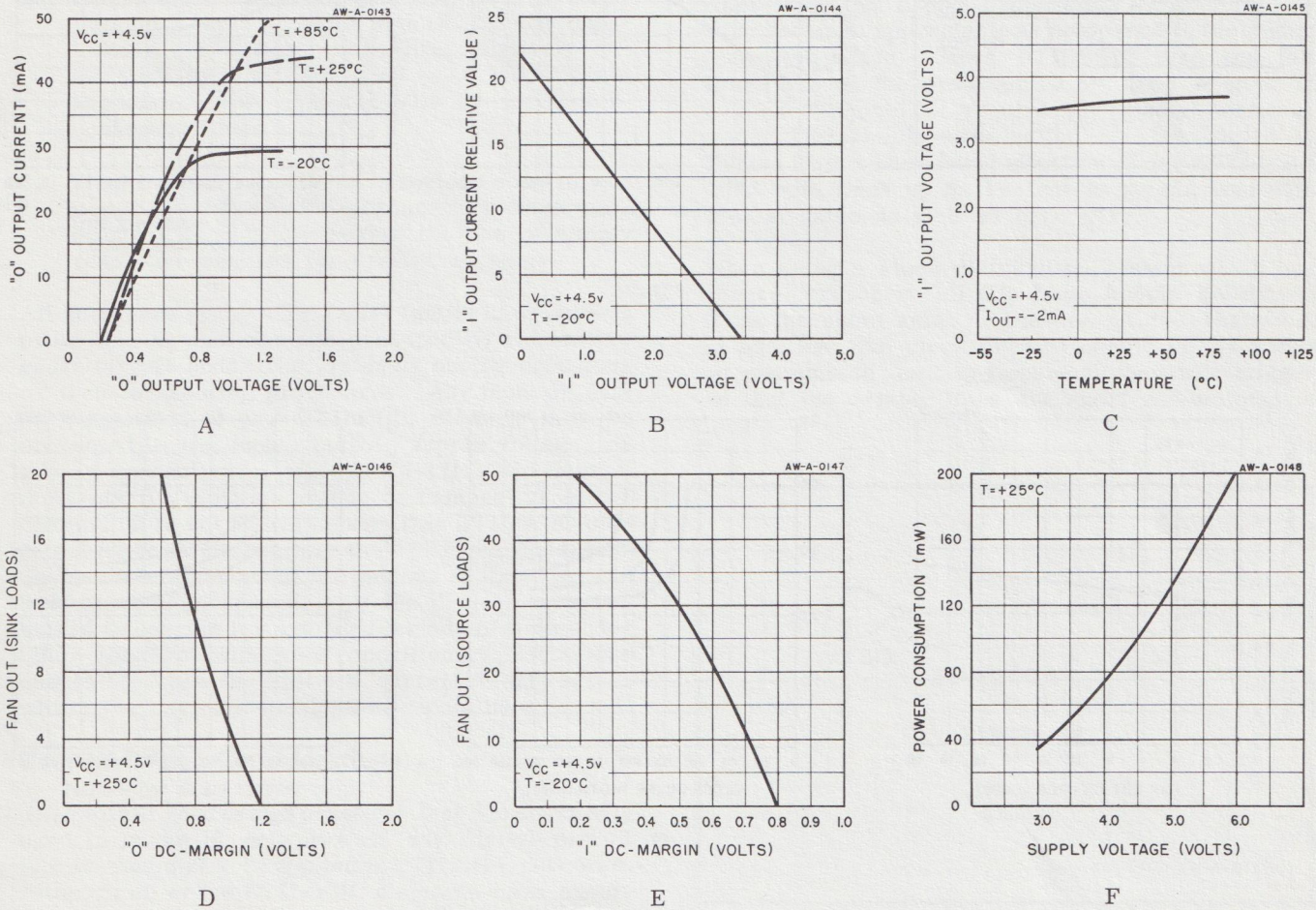
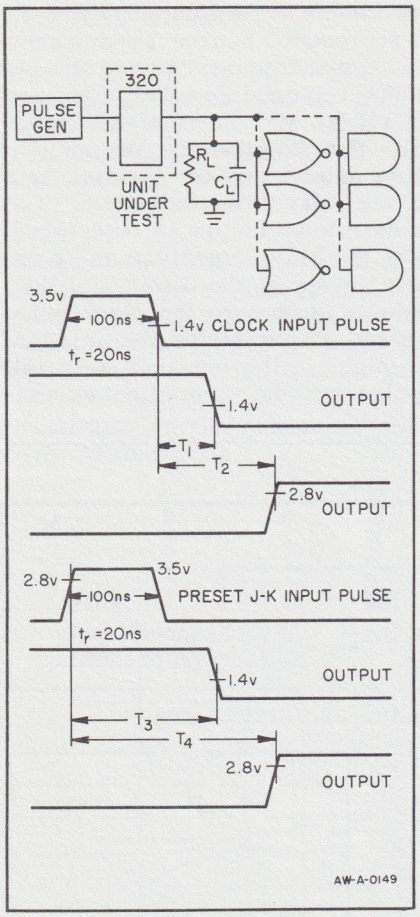
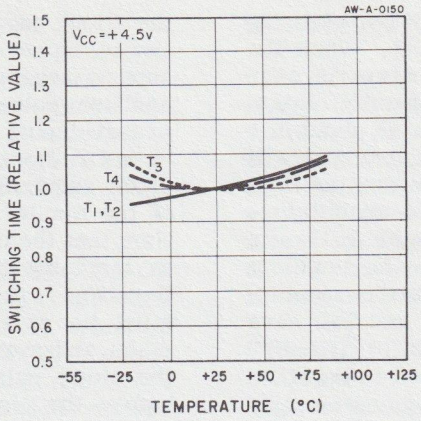


Figure 19 320 DC Characteristics



A



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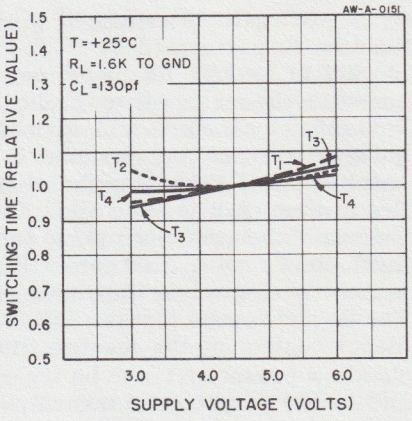

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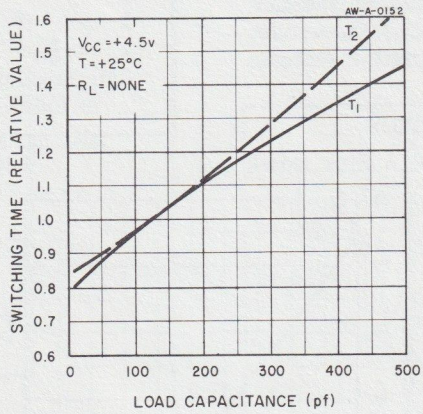
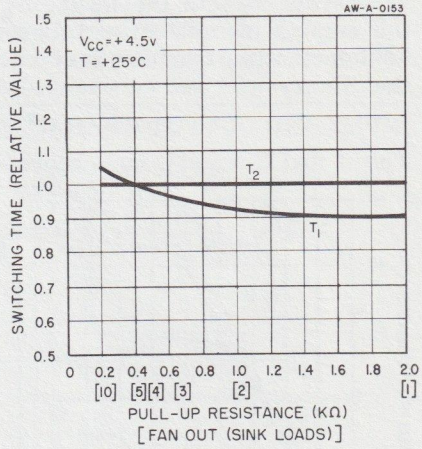


D



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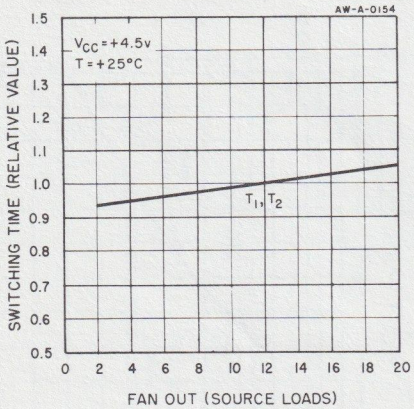

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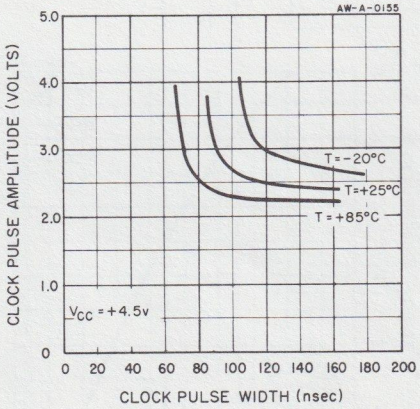

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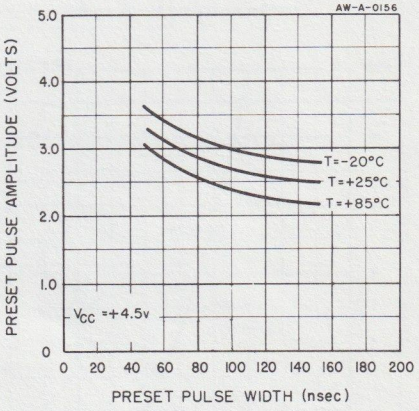


H

Figure 20 320 Switching Characteristics

HOW TO DESIGN WITH UTILOGIC

Information in this section gives examples of efficient system design with UTILOGIC integrated circuits. The use of the characterization curves presented earlier for each UTILOGIC circuit will be demonstrated here.

For example, the maximum operating frequency of a Modular Binary Counter is calculated. This calculation uses UTILOGIC characterization curves, suggesting a tabular form for design calculations. Interfacing is discussed, including the interconnecting of UTILOGIC and other circuit types. Typical interfacing techniques are illustrated.

Some of the features of UTILOGIC that make the family especially interesting to the systems engineer are:

1. High noise immunity, a major design consideration where application may be in high ambient noise environments that are encountered in industrial control equipment, computer peripherals, etc.

2. Low output impedance, essential for good noise immunity, also provides high DC fan-out capabilities. Switching times are relatively unaffected by the increased load capacitance associated with high fan-outs or long interconnecting lines.

3. Single power supply to provide economy in power supply costs. Tolerance to voltage variations (±10 percent) permit the use of simply regulated supplies for further economy.

All members of the UTILOGIC family have built-in protection against damage produced by momentary short circuit conditions, valuable during debugging or trouble-shooting procedures. Any input or output connection of any UTILOGIC element may be connected to the input, output, supply voltage, or ground connection of any other UTILOGIC element momentarily, without producing damage to either circuit. It is not recommended that UTILOGIC elements be connected so that they produce conditions designated as abnormal for periods of time that can be measured in seconds. If the devices are required to operate for extended periods of time under other than recommended conditions, precautions should be taken to limit the current to safe values within the device's dissipation capabilities.

General Design Considerations

The normal good design practices that are commonly used in layout of networks of any digital circuit family should also be applied to UTILOGIC networks. Although all of the UTILOGIC elements have excellent noise margins, any circuit, discrete or integrated, will produce erroneous results if the noise levels become high enough. As in any system, grounding, DC distribution, and noise problems should be considered from the very beginning of the design.

A major consideration with integrated circuits is the higher packaging density, as compared to discrete devices. For example, a printed circuit board that held 3 or 4 discrete flip-flops can now hold 30 to 40 integrated flip-flops; the design of the DC and ground distribution systems must allow for the corresponding current increases. DC and ground lines should be kept as short as possible and of adequate cross-section, and the use of tantalum or other high-frequency type by-pass capacitors is recommended.

The effect of the high circuit density on system cooling requirements and the increased possibility of localized hot spots must also be considered.

Signal leads should be kept as short as possible to minimize cross-talk, noise pick-up, and propagation time down the wire.

Generally, it becomes important to terminate signal lines when the signal propagation time down the wire becomes appreciable as compared to the signal transition times. Since UTILOGIC rise and fall times are on the order of 10 ns, lead lengths of 2 to 3 feet should not require any special termination. The simple termination network shown in Figure 21 has been found effective at any UTILOGIC input with lines up to 12 feet in length, and with coaxial cable as well as open wire.

When using a clock distribution system which has several branches, all flip-flops should be driven from the same relative position on the branches. In addition, the clock drivers should be as close as possible to the flip-flops that they will trigger so that the driving lines are short and uniform in length.

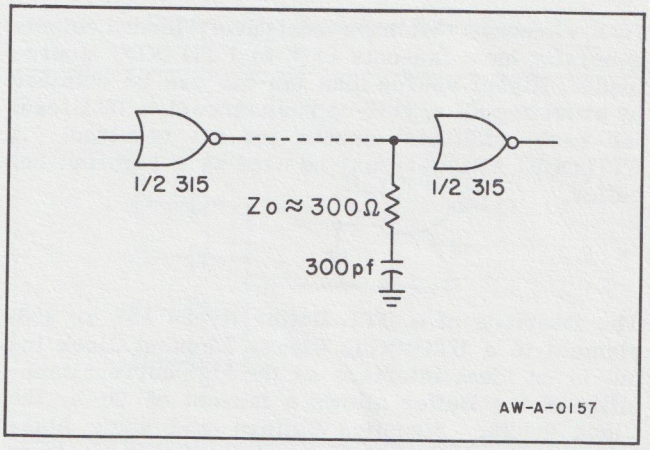


Figure 21 Termination Network

Interfacing Considerations

GENERAL CONSIDERATIONS

The need to interface UTILOGIC integrated circuits with discrete component circuitry or with integrated circuits of another family may arise when a UTILOGIC system or subsystem is added to or must operate with existing hardware. General rules when interfacing are:

1. Inputs to UTILOGIC source loads must be capable of supplying 140 μA input current at the "1" input threshold voltage of at least 2.7 volts.

2. Inputs to Sink Loads must be capable of sinking 2.1mA at the "0" voltage (0.6V).

3. A UTILOGIC output will supply 2mA at 3.3 volts for NORS, ORS, and Binary Elements, and 3.15 volts for ANDS.

4. The approximate equivalent circuit for any UTILOGIC output at "1" is 100 ohms to 3.5 volts. A NOR, OR and Binary Element output will sink 12mA at 0.6 volts or less.

UTILOGIC AND DTL

A UTILOGIC-to-Signetics 100 or 600 series DTL (DTL in general) interface requires, at most, modification of load definitions. The input resistor of the DTL NAND gate and the UTILOGIC AND are approximately the same value so that the DTL load is equal to a UTILOGIC sink load. The "1" and "0" levels at UTILOGIC outputs are fully compatible with DTL input requirements and vice versa.

DTL elements that have resistively loaded outputs generally have fan-outs of 2 to UTILOGIC source loads. Higher source load fan-out can be obtained by providing 8K of pull-up resistance (1/4 DTL load) for each additional source fan-out required. A UTILOGIC AND gate may be used as a high-fan-out buffer.

The interface of a DTL Buffer (types 157 or 659) element to a UTILOGIC Binary Element Clock input is an ideal interface as the high current capability of the Buffer allows a fan-out of 20 to the Clock inputs. Signetics Buffers (and some high-fan-out gates e.g., 113) are also suitable for lamp driving.

Mixed UTILOGIC — DTL systems should operate with a 4.5 volt power supply; the rules above assume a common power supply.

UTILOGIC TO RTL

The Resistor-Transistor (grounded-emitter transistor amplifier) logic stage, Figure 22, is often employed as a level translator or general purpose buffer stage since all that is required generally is one transistor and one or two resistors. At these interfaces, the output of a UTILOGIC element may be treated as voltage source of +3.5V (less than 100 ohms source impedance). For a typical input current requirement of 0.5mA, R_{in} in Figure 22 will be 5KΩ.

MISCELLANEOUS INTERFACES

For applications where input "1" levels are higher than UTILOGIC "1" levels ("0" voltages about equal), several interfacing possibilities exist. A UTILOGIC AND gate may be used as a buffer by using a series diode (d) to improve the input breakdown voltage (see Figure 23). The external resistor, (R), may be used to improve the "0" offset voltage, thereby compensating for the voltage rise across the diode (each 20KΩ load reduces fan-out by 1). High conductance diodes are recommended to keep the input voltage as low as possible.

Interfacing high "1" voltage outputs to UTILOGIC source load inputs may be accomplished by techniques such as those in the following four examples. In Figure 24, the forward voltage of one or more diodes is the voltage dropping medium. In Figure 25, a zener diode is used when voltage drops of 5 volts or more must be obtained. The resistor, R, may be used to increase the zener current to improve its regulation. Using a zener as shown in Figure 26, may be especially desirable if the "1" level of the driving source has large variations. In Figure 27, a simple resistive voltage divider provides the necessary voltage reduction, and may be used when minor modifications to the logic levels are required and when high speeds are not necessary.

When the "1" level output of another logic circuit will not reach the required UTILOGIC input level of 2.7 volts, the 316 or 331 Expandable gates will often provide an acceptable buffer, shown in Figure 28. Because the voltage required to switch an Expandable Gate is a "diode drop" lower at the Expansion Input than at the regular inputs, "1" levels of 2.0 volts and "0" levels of 0.8 volts are sufficient. Maximum "1" input current is 3mA. This Expansion Input interface scheme also may be used at interfaces with Diode Logic, shown in Figure 29.

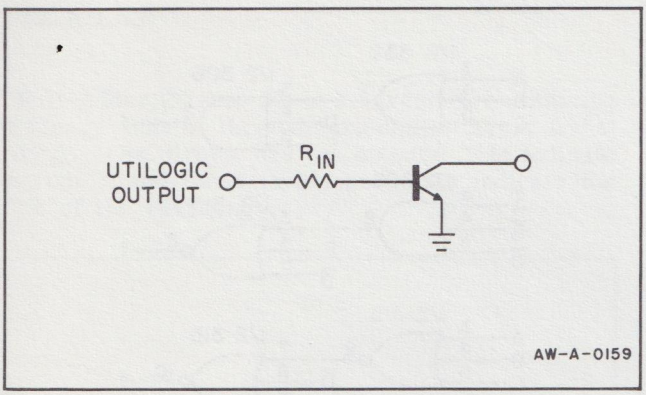


Figure 22 UTILOGIC to RTL Interface

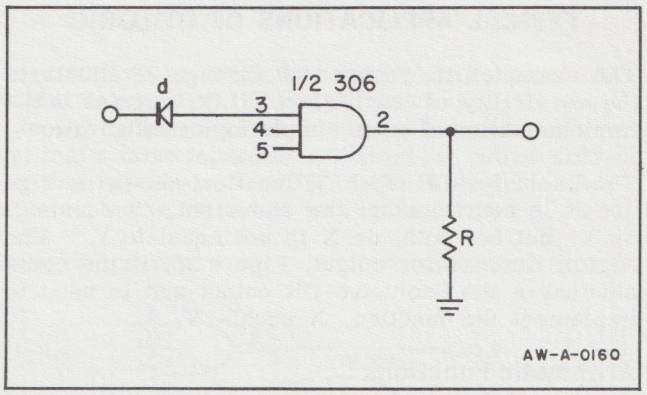


Figure 23 High Level to AND Interface

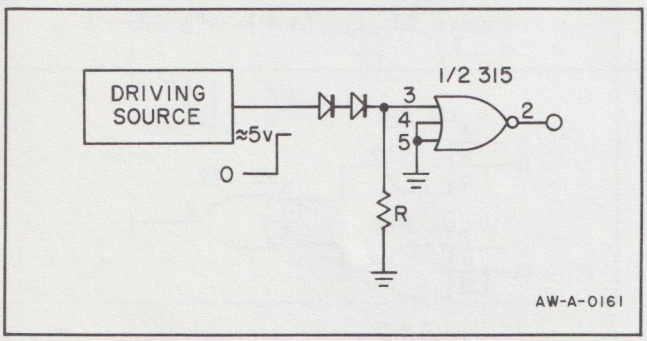


Figure 24 5 Volt to Source Input Interface

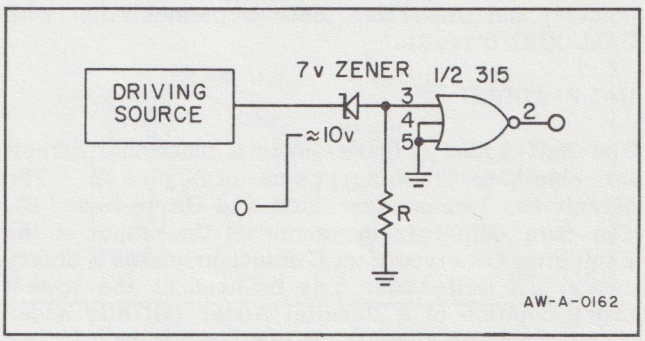


Figure 25 10 Volt to Source Input Interface

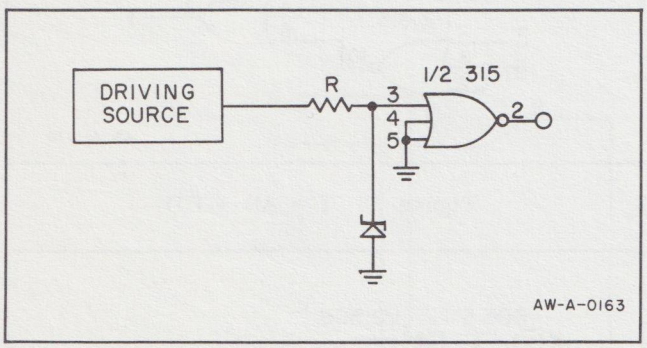


Figure 26 Interfacing with Variable Input Levels

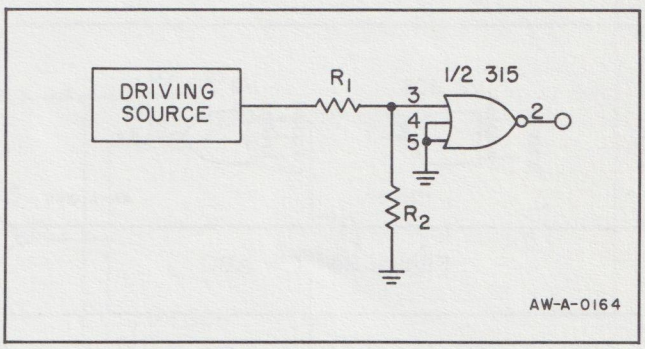


Figure 27 Resistive Interface

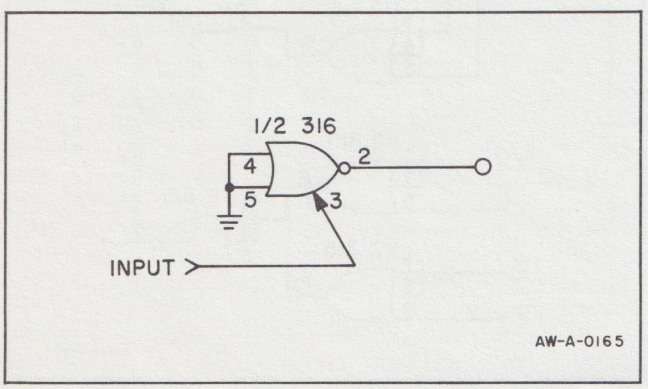


Figure 28 Low Level to UTILOGIC Interface

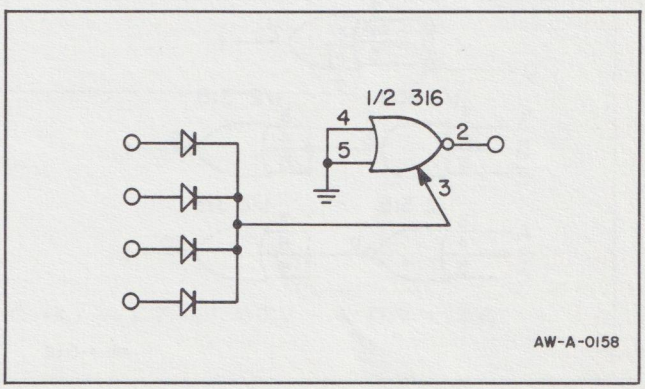


Figure 29 Diode Logic to UTILOGIC Interface

TYPICAL APPLICATIONS OF UTILOGIC

The examples in Figures 30 through 38 illustrate the versatility of the basic UTILOGIC gates in the implementation of some simple logic configurations.

The Exclusive-OR (X ⊕ Y) function, shown in Figure 34 is equivalent to the statement, "f equals X or Y, but not both, or X is not equal to Y." The Digital Comparator output, Figure 35, is the complement of the Exclusive-OR output and is used to implement the function, X equals Y.

Arithmetic Functions

This subsection describes three basic arithmetic functions (Half-Adder, Full-Adder, and Full Subtractor) and illustrates their implementation with UTILOGIC circuits.

HALF-ADDER

The Half-Adder (Figure 36) is a functional circuit for obtaining the binary sum of X plus Y. The circuit has two outputs, Sum and Carry (S and C). The Sum output is the same as the output of the Exclusive-OR circuit; the C output indicates a binary carry. A Half-Adder may be used at the lowest order position of a Parallel Adder (all bits added simultaneously) since there is no carry input to this position. Two Half-Adders may be combined to obtain a Full-Adder.

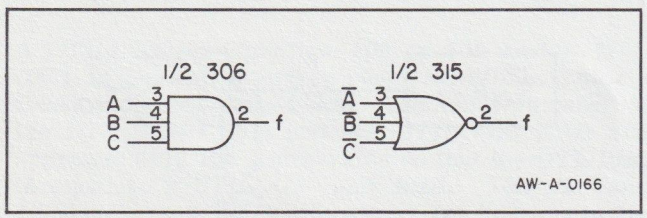


Figure 30 f = ABC

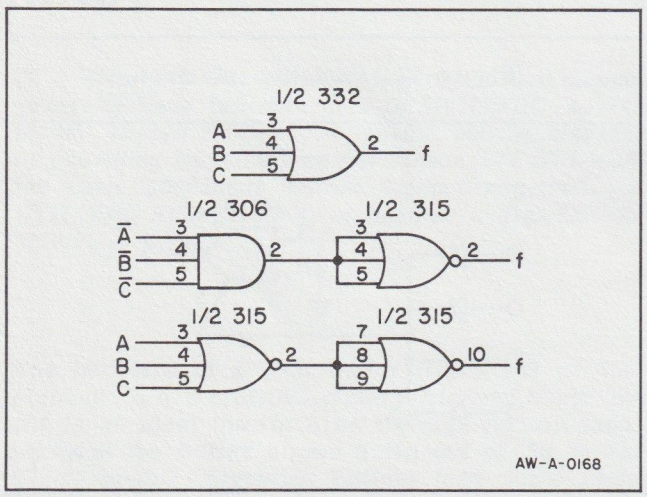


Figure 31 f = A + B + C

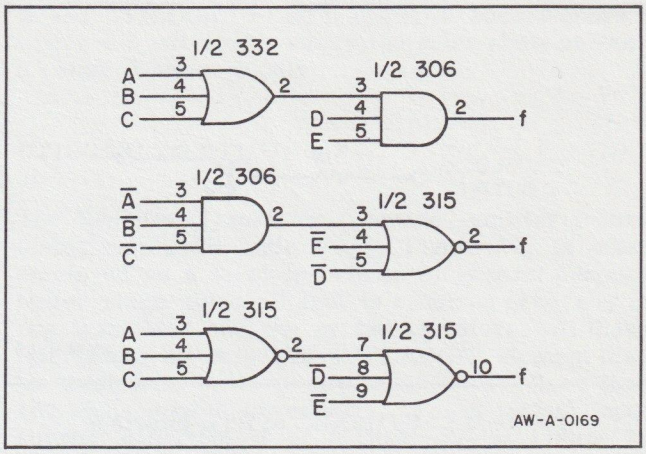


Figure 32 f = (A + B + C) DE

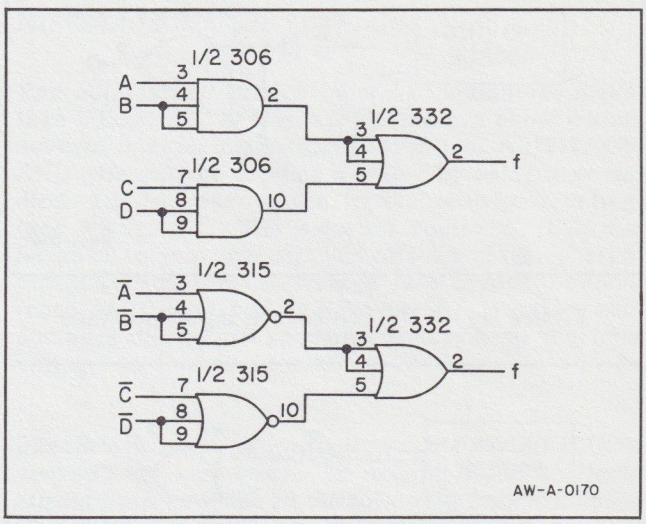


Figure 33 f = AB + CD

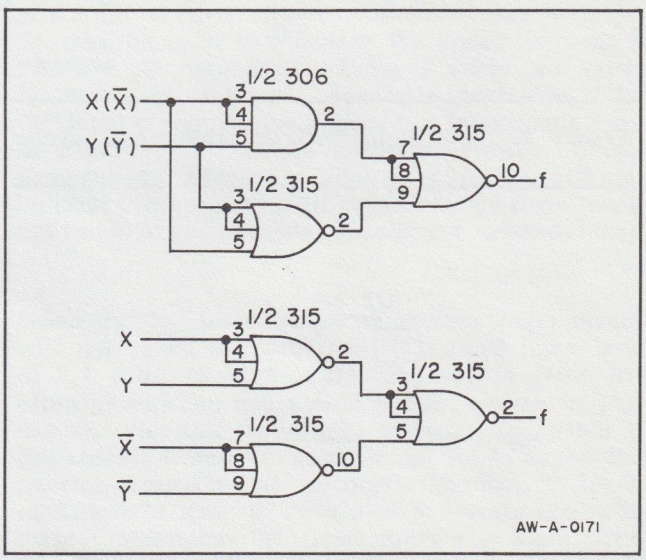


Figure 34 Exclusive-OR

FULL ADDER

A Full-Adder (Figure 37) is a circuit for obtaining the binary sum of three binary digits, X, Y, and C (carry). The circuit has two outputs: S to indicate the sum of the three inputs and C' to indicate the value of the resulting carry.

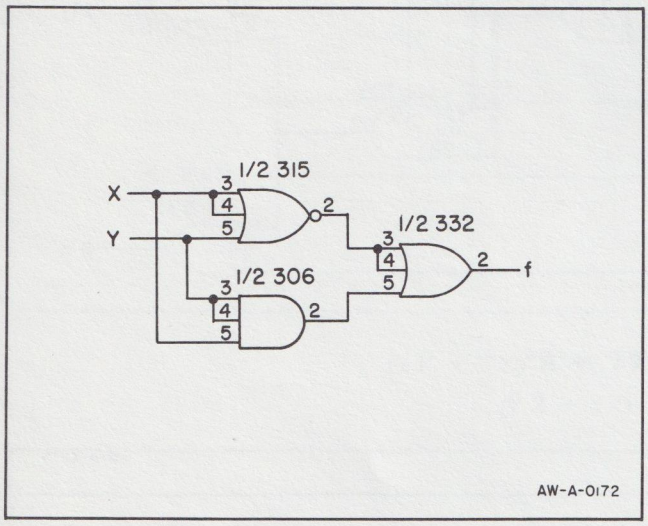


Figure 35 Digital Comparator

FULL SUBTRACTOR

The circuitry to obtain the binary Difference, (D equals X minus Y minus Borrow), and B' (new Borrow), is identical to the above Full-Adder, except that a false input and a change of output notation are required. The UTILOGIC Full Subtractor implementation is shown in Figure 38.

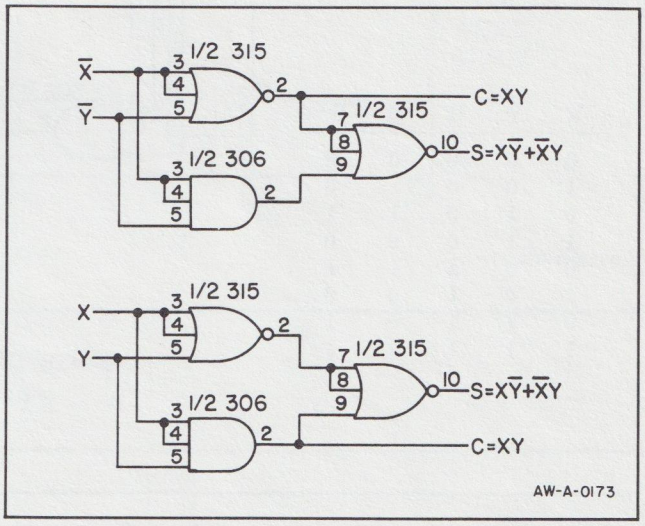
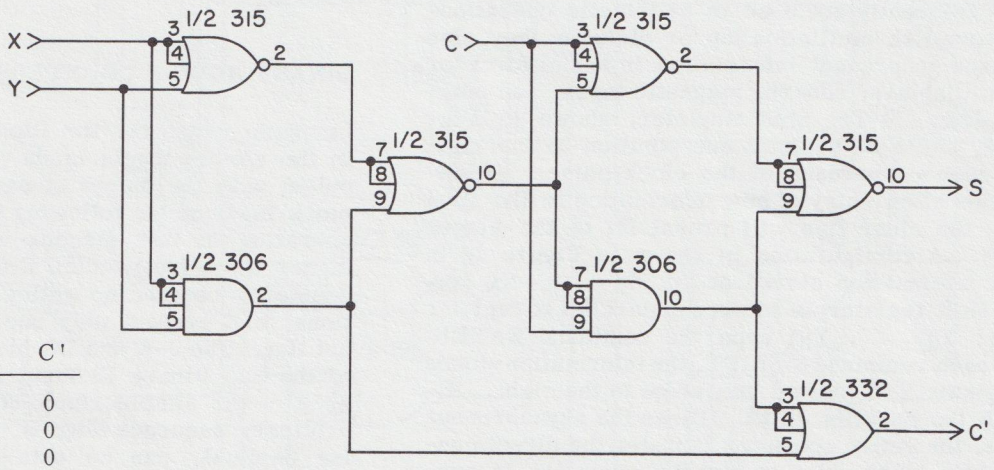


Figure 36 Half Adder

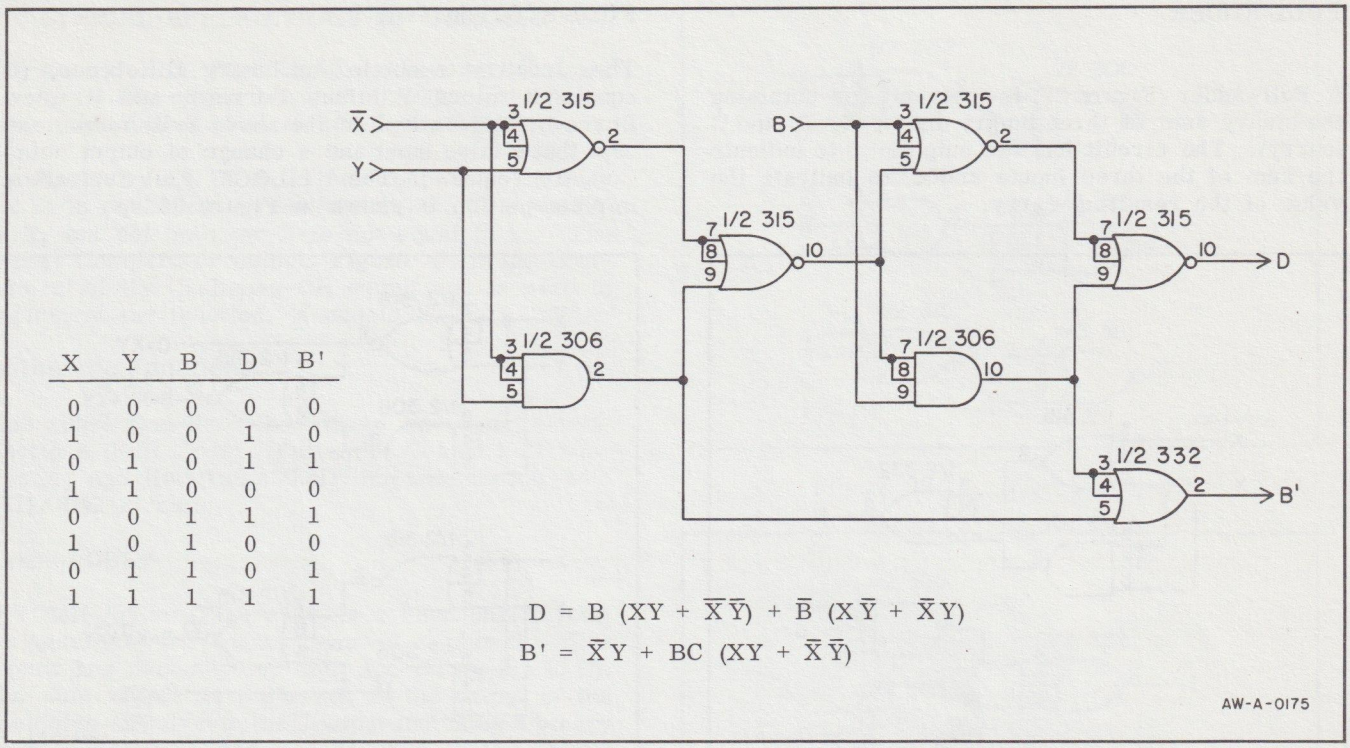


X	Y	C	S	C'
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

$S = C\,(XY + \bar{X}\,\bar{Y}) + \bar{C}\,(X\bar{Y} + \bar{X}\,Y)$ $C' = XY + C\,(X\bar{Y} + \bar{X}Y)$

AW-A-0174

Figure 37 Full Adder



X	Y	B	D	B'
0	0	0	0	0
1	0	0	1	0
0	1	0	1	1
1	1	0	0	0
0	0	1	1	1
1	0	1	0	0
0	1	1	0	1
1	1	1	1	1

$$D = B\,(XY + \overline{X}\,\overline{Y}) + \overline{B}\,(X\overline{Y} + \overline{X}Y)$$

$$B' = \overline{X}Y + BC\,(XY + \overline{X}\,\overline{Y})$$

Figure 38 Full Subtractor

Shift Registers

A Shift Register is a circuit for storing and shifting a number of binary or decimal digits. Shift Registers frequently are used in arithmetic operations to accomplish multiplication or division; they also are used to present information in serial form for use in displays, adders, magnetic tapes, and magnetic drums. The Shift Register, shown in Figure 39, shifts its contents one position to the right upon each occurrence of the clock pulse. The input lines allow entry of new information to the first stage; the clear line will preset all of the stages to "0". A configuration is shown in Figure 40 in which information stored at X_1, X_2 . . . X_N (another shift register) is entered in parallel to register Y (Y_1, Y_2 . . . Y_N) upon the command ENTER. Upon each command to SHIFT, the information stored in register Y is shifted one stage to the right. Although the parallel entry utilizes the asynchronous inputs, the entire operation is under the direct control of the clock pulse so that the operation is synchronous.

Counting Functions

Since many computing functions, such as indexing and program control, are essentially counting functions, a large variety of counters is used in computing equipment. Some of the more common counter types discussed in this section showing the flexibility of the UTILOGIC family are: asynchronous ripple counters, useful for frequency division; simple synchronous counters for high-speed logic operations; reversible counters for specialized control; and feedback shift registers which are especially suited for commutation and very high-speed counting.

BINARY RIPPLE COUNTERS

In ripple counters, the flip-flop normally operate in the simple toggle mode (change with each clock pulse) with the output of each element driving the clock input of the following stage. Ripple counters operating in this manner are able to operate at higher input frequencies than most other types of counters, require no gating and few interconnections, and present only one clock input to the input line. The J-K and DC clock line characteristics of the 320 Binary Element allow the binary sequence of the simple ripple counter to be modified to arbitrary sequence lengths, many of which, including decimal, can be obtained without gating. A limitation of all ripple counters is that a change of state may be required to ripple through the entire length of the counter. The propagation time of this change may determine the maximum operating frequency of the modified types and will determine when any decoding networks may be sampled. A simple Binary Ripple Counter that counts up is shown in Figure 41. Since each stage changes state (complements) on each "1" to "0" transition of the previous stage, the counter is implemented by connecting the clock input of each stage to the "Q" output of the previous stage.

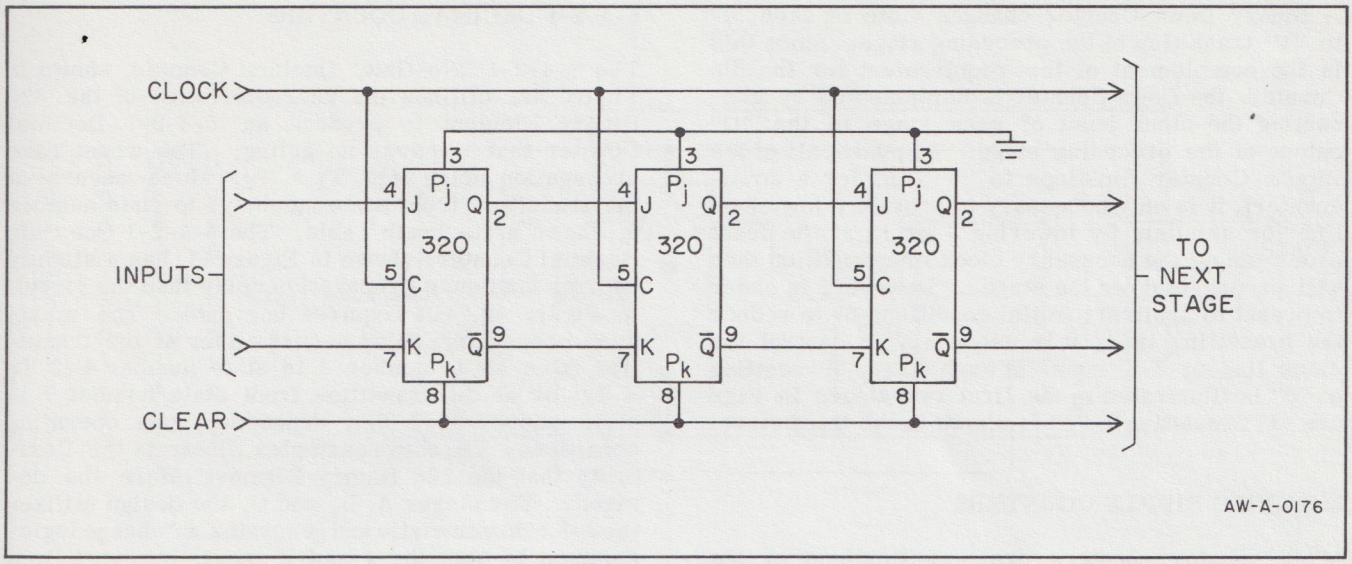


Figure 39 Shift Register

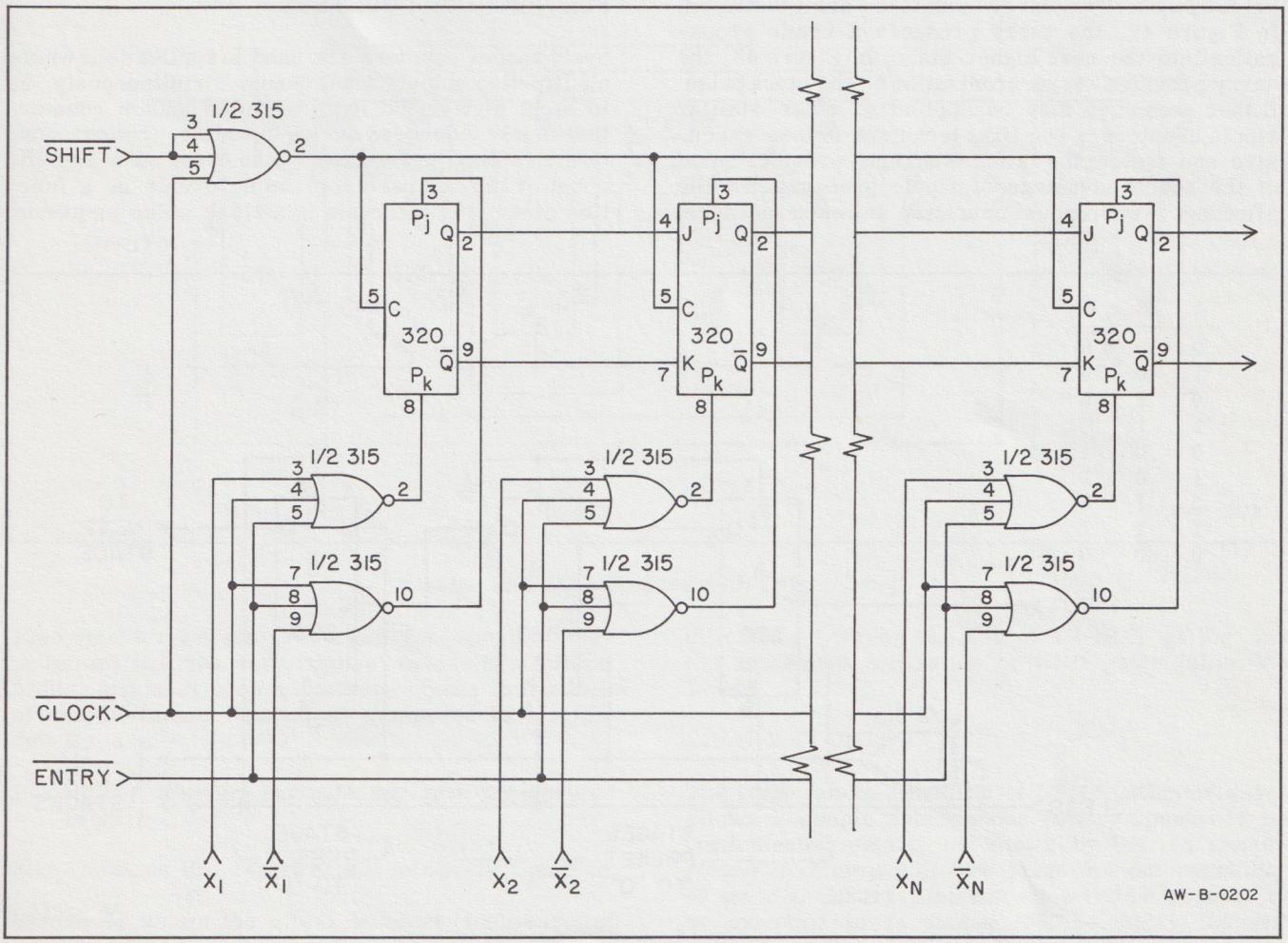


Figure 40 Parallel Entry Shift Register

A Binary Down Counter changes state on each "0" to "1" transition of the preceding stage. Since this is the complement of the requirement for the Up Counter, the Down Counter is implemented by connecting the clock input of each stage to the "$\bar{Q}$" output of the preceding stage. To preset all of the Ripple Counter flip-flops to "0" ("1" for a down-counter), it is only necessary to provide a low clock line (or simulate by lowering J or K) at the least order stage; the necessary clock line condition then will propagate down the stages. However, in order to preset to arbitrary initial conditions or to reduce the presetting time, it is necessary to control the clock line or J-K inputs at each stage. Presetting to "0" is illustrated in the first two stages in Figure 41; presetting to "1" is shown in the third stage.

MODIFIED RIPPLE COUNTERS

Many popular counters are modifications of the basic Binary Ripple Counter previously described. The decimal counter modifications, shown in Figures 42 and 43, illustrates the versatility obtained by combining the ripple counting technique with logical feedback. Two carry techniques are illustrated. In Figure 42, the carry produces a ripple propagation into the next higher stage; in Figure 43, the carry provides resynchronization to the clock pulse. Either technique may be applied to other similar ripple counters. The first technique is less expensive and faster; the latter technique provides most of the speed advantage of ripple propagation while allowing synchronous operation between decades.

8-4-2-1 DECIMAL COUNTERS

The 8-4-2-1 "No-Gate" Decimal Counter, shown in Figure 42, utilizes the characteristics of the 320 Binary Element to produce an 8-4-2-1 Decimal Counter that requires no gating. The worst case propagation delay is 3 T_1 + T_2, which occurs at the transition from state number 7 to state number 8, shown in its Truth Table. The 8-4-2-1 One Gate Decimal Counter, shown in Figure 43, has a slightly shorter maximum propagation delay than the circuit in Figure 42, but requires one gate. The maximum propagation delay occurs either at the transition from state number 3 to state number 4 (2 T_1 + T_2) or at the transition from state number 7 to state number 8 (3 T_1), depending upon operating conditions. The above examples illustrate the flexibility that the 320 Binary Element offers the designer. For stages A, B, and C, the design utilizes the J-K characteristic and generates a "change logic" common to both the J and K input. At stage D, it is more economical to treat the 320 as an R-S flip-flop and to generate independent "set" and "reset" logic.

SYNCHRONOUS COUNTERS

Synchronous counters are used in applications where all flip-flop outputs must change simultaneously, as in most high-speed logic systems and in counters that must be decoded during counting. Synchronous counters may be used to stop an event on a specific count or may be used for timing events as a function of specific intervals in a clock pulse sequence.

A	B	C
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
0	0	0

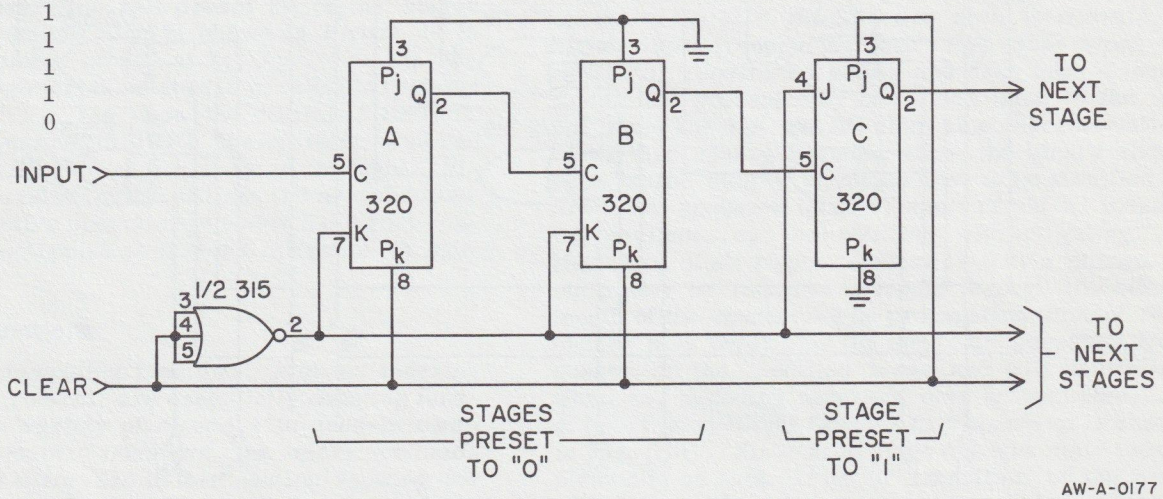


Figure 41 Binary Ripple Counter

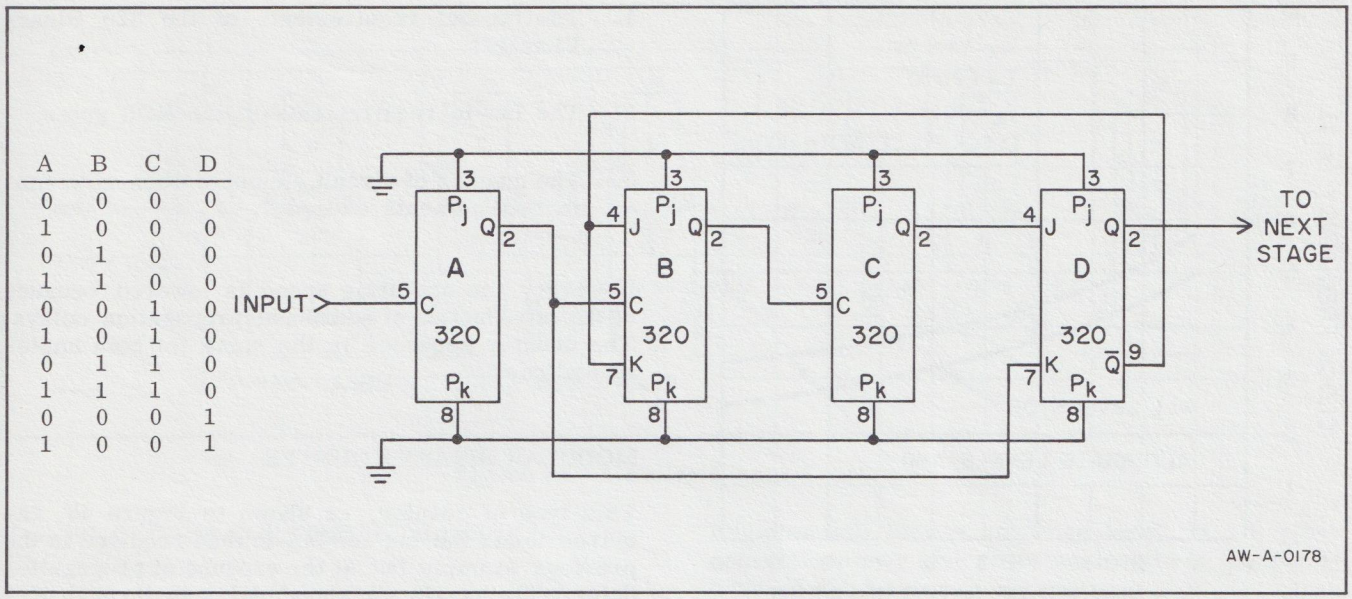


Figure 42 Decade (BCD) Counter "No Gate"

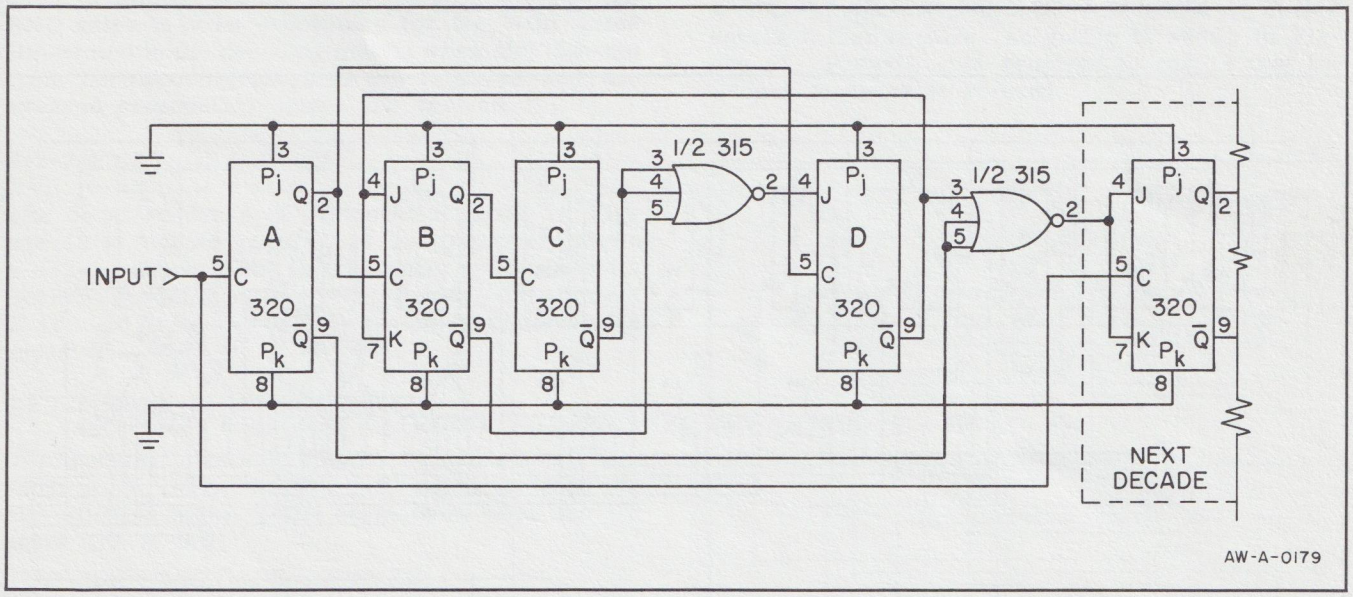


Figure 43 BCD Counter with Gated Carry

Also, these counters are useful for special computer applications that involve reversing, special codes, and start/stop operations. Some limitations of a synchronous counter as compared to a ripple counter are:

1. Higher flip-flop fan-outs and gate fan-ins are required.

2. The clock line represents a relatively high load.

Figure 44 shows the effect on clock frequency of an increasing number of gates between binaries in any synchronous system; the two curves show the difference between the use of all-NOR gating and the maximum utilization of AND gates (alternate levels).

BINARY COUNTER

The large fan-in capability of UTILOGIC NOR gates allows a simple Synchronous Binary Counter to be implemented easily, as shown by the ten sample stages in Figure 45. The large fan-out capability of the 320 Binary Element allows this counter to be extended to 14 stages (16,384 states) without buffering. The alternate implementation shown reduces:

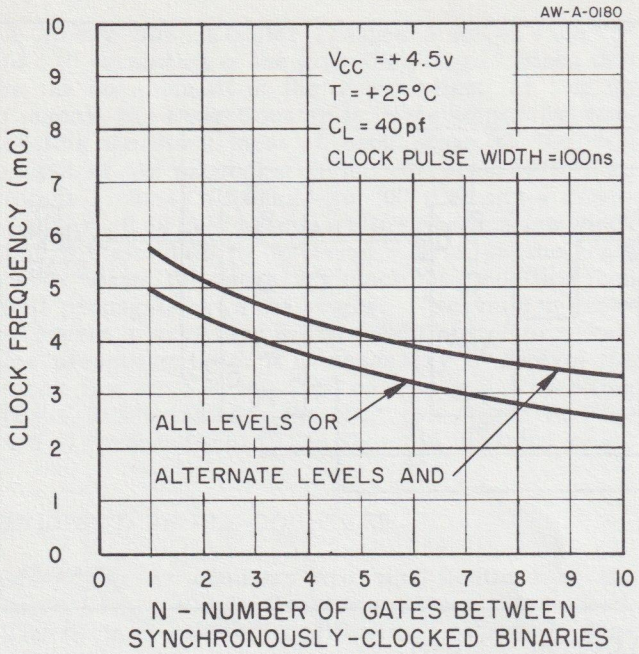


Figure 44 Effect of Logic Depth on Clock Frequency

1. The fan-out requirements of the 320 Binary Elements.

2. The fan-in requirements of the NOR gates.

3. The number of circuit elements when gate fan-in requirements exceed 7.

However, the operating speed is lowered because of the introduction of additional propagation delays. The counter sequence is the same for both implementations.

MODULAR BINARY COUNTER

This type of counter, as shown in Figure 46, requires lower fan-out and fan-in than required in the previous example but at the expense of propagation delay. The maximum signal delay is through N-2 gates for a counter of N stages. Stages may be added in a modular fashion because the logic is repetitive for each stage.

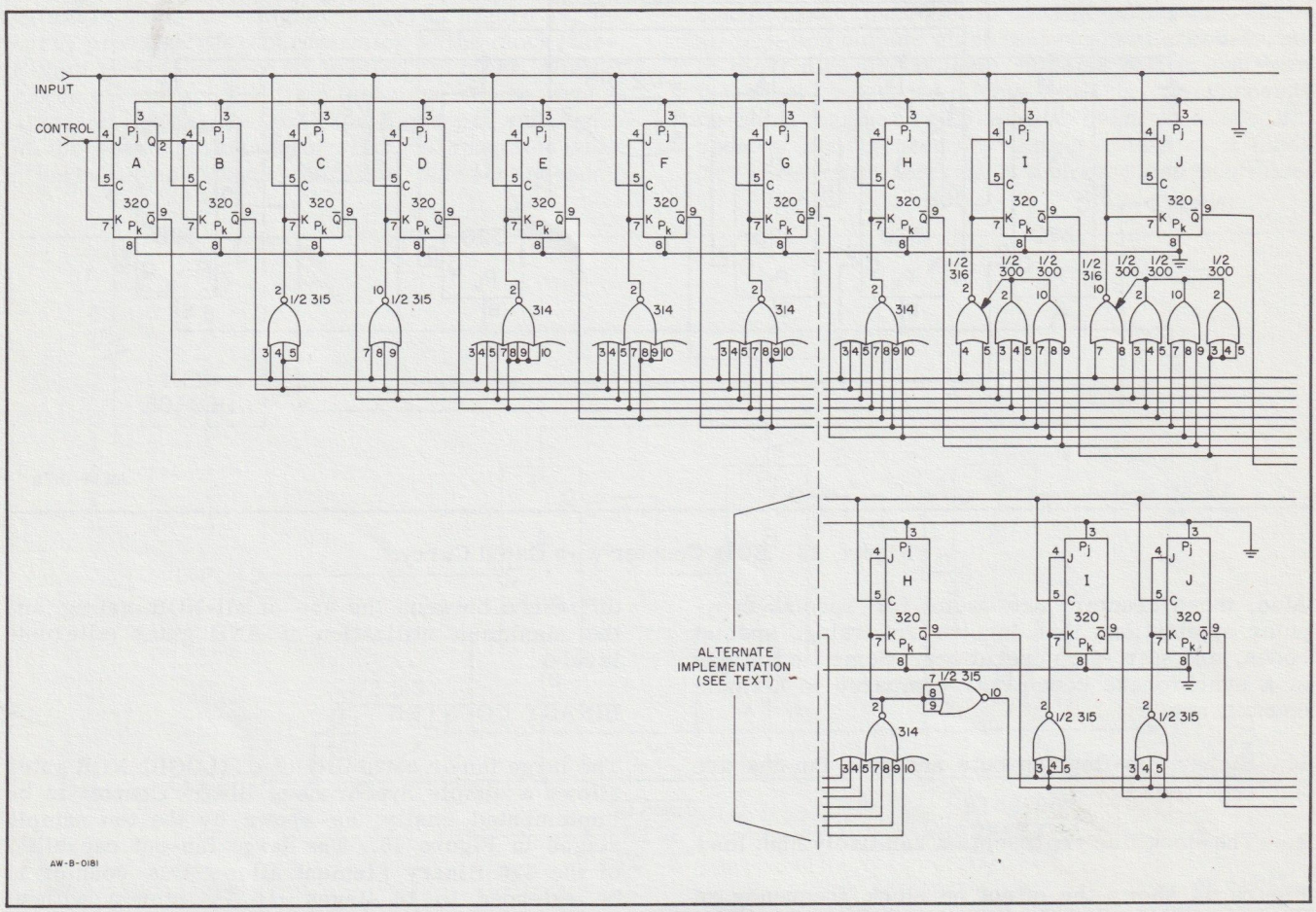


Figure 45 Synchronous Binary Counter

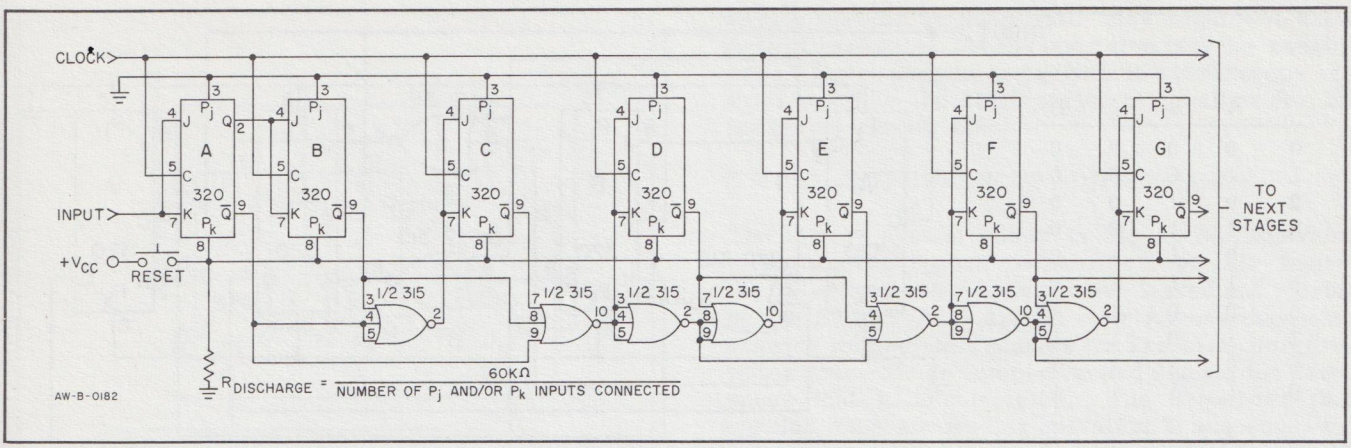


Figure 46 Modular Binary Counter

8-4-2-1 DECADE COUNTER WITH DECIMAL DECODING

Feedback and the J-K characteristics of the UTILOGIC 320 are employed to produce the 8-4-2-1 decade counter shown in Figure 47. UTILOGIC AND gates may be substituted for the NOR gates illustrated in the decoding matrix when sink fan-out from the decoding gates is not required and decreased propagation delays are desired.

4-2-2-1 DECADE COUNTER

The count sequence of the counter shown in Figure 48 is not as popular as the previously shown 8-4-2-1 sequence but is frequently used since its decimal decoding matrix requires only 3-input gates. It is used quite extensively in the instrumentation industry.

REVERSIBLE BINARY COUNTER

The counter shown in Figure 49 will count every input pulse. The counter will count up when the UP input is high; it will count down when the UP input line is low.

REVERSIBLE DECADE COUNTER

The counter shown in Figure 50 uses feedback to produce an 8-4-2-1 decade sequence. The counter will count only when the appropriate command is present.

FEEDBACK SHIFT REGISTERS

Feedback Shift Registers or Ring Counters, like the ripple-carry counters, are capable of operating at the maximum frequency of the flip-flops; they have the additional feature of being able to shift as well as count. This characteristic is very valuable when the information in the counter is to be presented as a serial word to a display or memory device. When connected as a Ring Counter, a Feedback Shift Register will have a sequence length of 2N; other connections may give sequence lengths to the maximum of 2^N-1.

Simple Ring Counter

A very simple Ring Counter with sequence of 6 (N equals 3) that requires no gating is shown in Figure 51. Presetting is required to ensure that the proper sequence is entered.

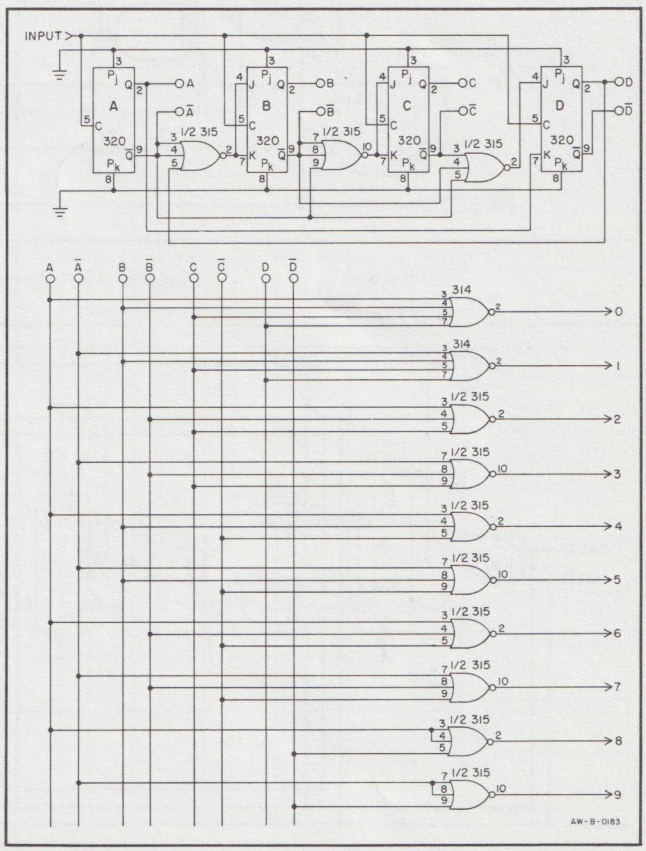


Figure 47 BCD Counter with Decimal Decoding

	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	1	1	0
5	1	1	1	0
6	0	0	1	1
7	1	0	1	1
8	0	1	1	1
9	1	1	1	1

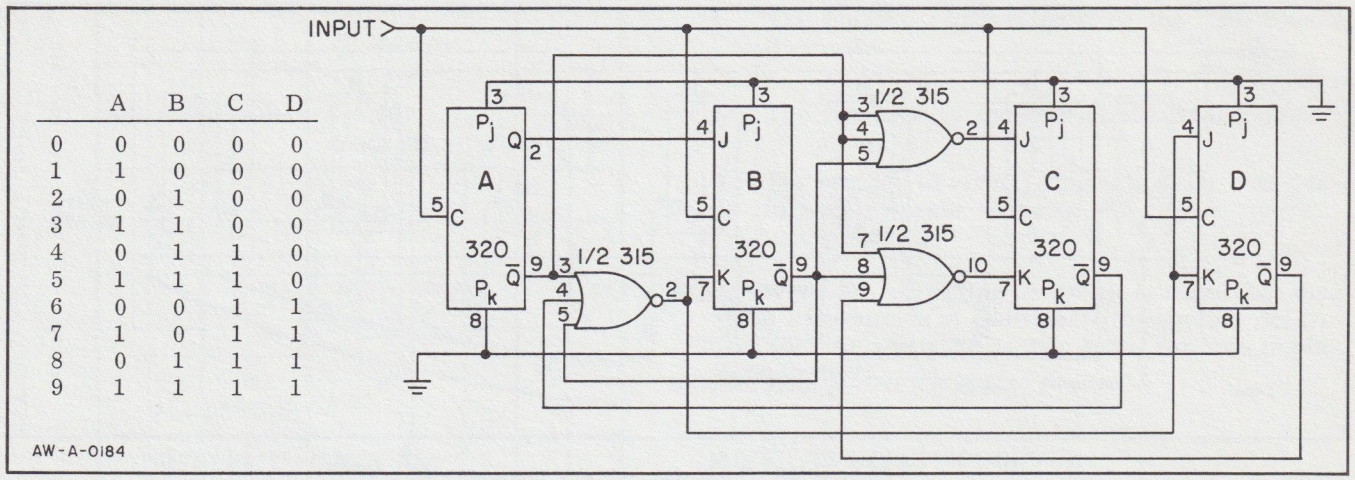


Figure 48 4-2-2-1 Decade Counter

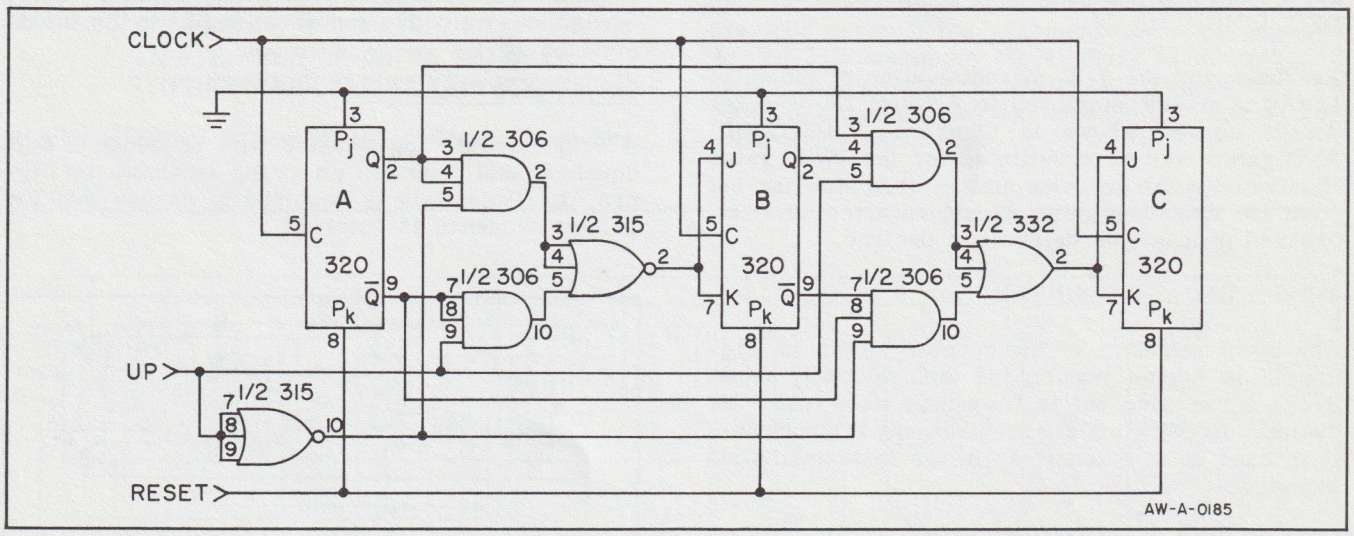


Figure 49 Reversible Binary Counter

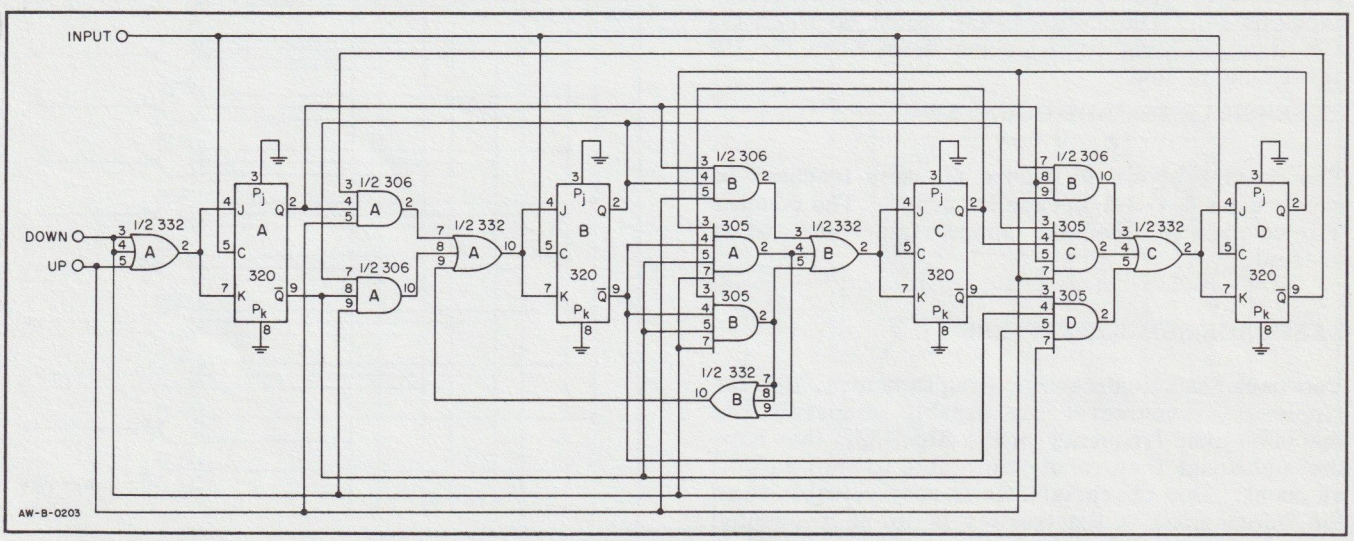
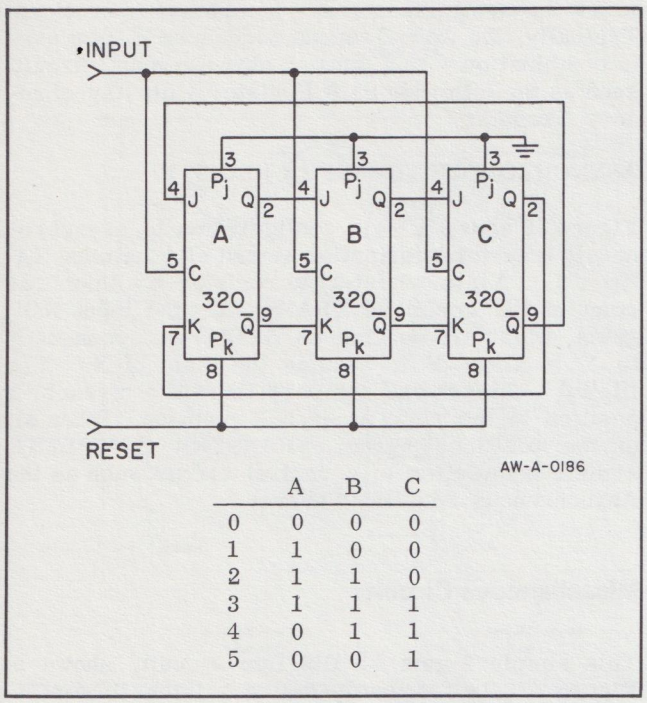


Figure 50 Reversible Decade Counter



	A	B	C
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1

Figure 51 Simple Ring Counter

Decimal Ring Counter With Decoding and Self-Sequencing

The counter in Figure 52 is essentially the above counter except that N equals 5, and a gate has been added to provide self-sequencing. Readout gating is shown to illustrate its simplicity. UTILOGIC AND gates may be substituted for the NOR decoding gates when sink fan-out from the decoding gates is not required, and decreased propagation times are desired.

Johnson Counter

The Johnson Counter (Feedback Shift Register) has a sequence length, 2^N-1, for most small N (N equals the number of stages). However, for some N, the sequence lengths may be different. For example, when N equals 5, one initial state (00000) gives 21 states; another (11000) gives 7; a third initial state (00100) gives 3 states. The Johnson Counter can be designed to produce sequence lengths not easily obtainable with other high-speed counter designs; however, this type of counter is hard to decode and debug since there is no common pattern to the sequence. The Johnson Counter shown in Figure 53 has a sequence length of 15 (initial state "0000") as shown in the Truth Table.

Asynchronous Control Configurations

In the following asynchronous examples, the timing of the operations is controlled by internally generated signals instead of by an external clock source as in synchronous operations. The logic required to generate the timing signals may require a great deal of hardware, but the operation may be considerably faster than in an equivalent synchronous operation where the clock period must allow for the maximum circuit delays.

SIMPLE ASYNCHRONOUS ADD SEQUENCE

The simple system shown in Figure 54 illustrates typical asynchronous techniques. In this figure, the Asynchronous Sequencer is cleared and started by the START ADD signal. The Asynchronous Sequencer immediately enables the Transfer operation, which proceeds to completion and signals the Sequencer that it is completed. The Sequencer then enables each succeeding operation in sequence, but only after receiving a completion signal from each signal from each previous operation. After all operations under the control of the Sequencer have been completed, an ADD COMPLETE signal is sent to the master control circuits.

ASYNCHRONOUS SEQUENCER

The circuit shown in Figure 55 will generate the enable signals for "N" asynchronous operations. The Sequencer may be expanded where shown in

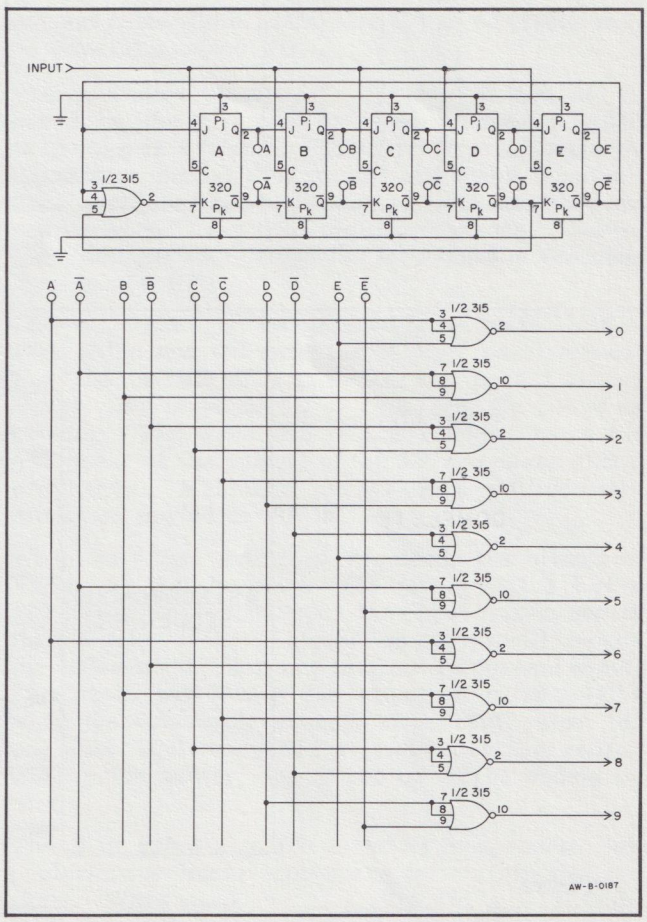
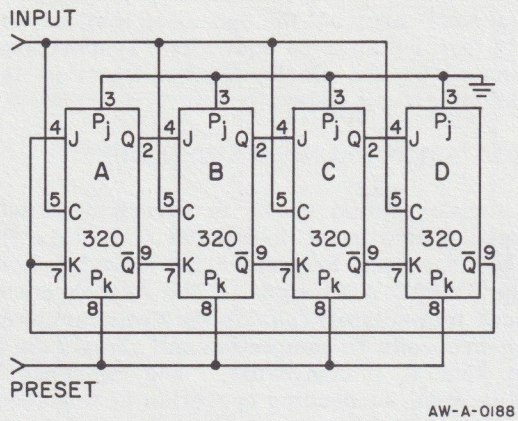


Figure 52 Decimal Ring Counter



	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	0	1	0	1
5	0	0	1	0
6	1	0	0	1
7	1	1	0	0
8	0	1	1	0
9	1	0	1	1
10	1	1	0	1
11	1	1	1	0
12	0	1	1	1
13	0	0	1	1
14	0	0	0	1
0	0	0	0	0

Figure 53 Johnson Counter

order to accommodate any number of operations. Typically, the Asynchronous Sequencer will be used in combination with a similar asynchronous circuit, such as the following Shift Register with Asynchronous Transfer.

ASYNCHRONOUS TRANSFER REGISTER

Figure 56 shows a logic configuration to asynchronously transfer information stored at locations X_A, X_B . . . X_N (a register) to register Y. Upon receipt of the command TRANSFER, the input NOR gates, which are serving as ANDS, will connect X to Y to allow Y to assume the state of X. The Digital Comparators compare the state of each Y position to the state at each X position. When all of the positions agree, TRANSFER COMPLETE signals completion to a control circuit such as the Asynchronous Sequencer above.

Miscellaneous Circuits

This simple 2-gate RS flip-flop circuit, shown in Figure 57, is frequently called a latch to distinguish it from a more complex flip-flop, such as the 320.

The high input impedance of the UTILOGIC source inputs makes them ideally suited for use with integrating circuits to form a great variety of pulse-shaping circuits. When connected as in Figure 58, a Pulse-Width Discriminator is formed with a pulse-width threshold of about C_T where time is ns and C_T pf. By reversing the polarity of the diodes as in Figure 59, a simple Pulse Stretcher is formed. This circuit will widen positive pulses by about $8\,C_T$.

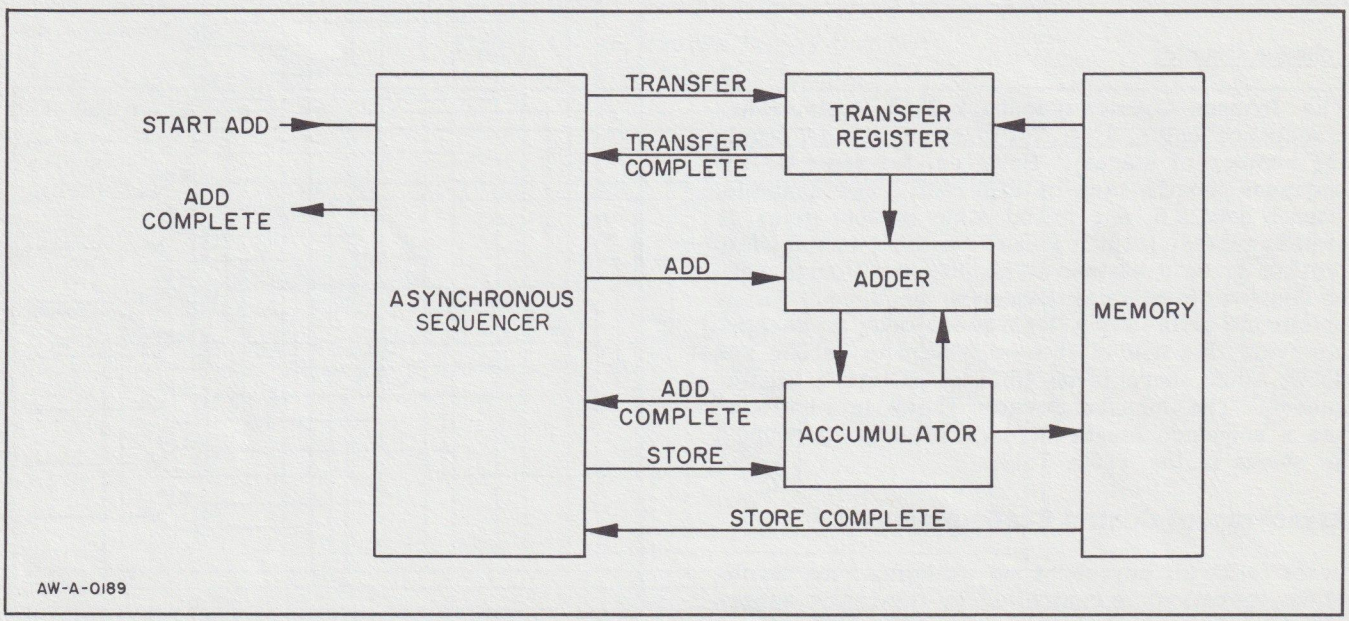


Figure 54 Asynchronous System

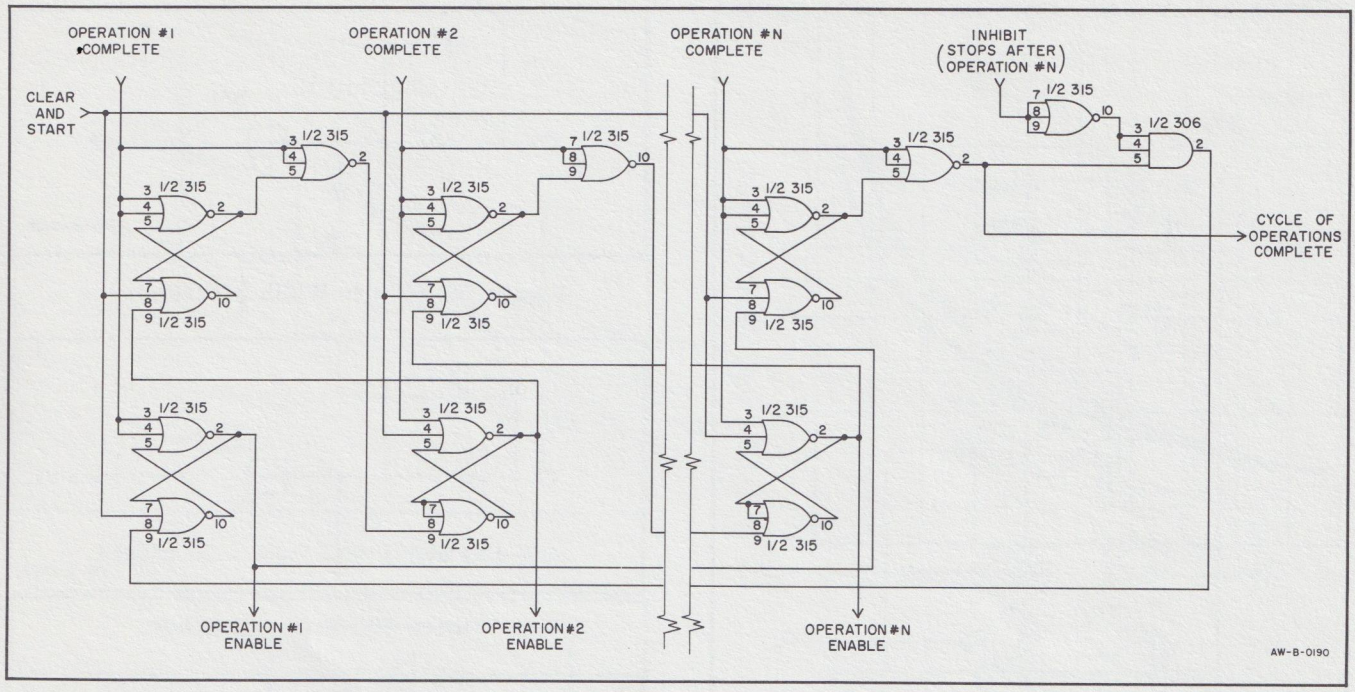


Figure 55 Asynchronous Sequencer

By integrating the output of a 320 and feeding the result to a preset input, a simple One-Shot with a period of 0.7 $C_T R_T$ is formed (Figure 60). The maximum period is about 1 millisecond with minimum periods on the order of 150 ns. R_T should be 5K or less. Some inductance in the feedback circuit is necessary to prevent oscillations at the end of the output pulse. In compact design, the inductance may be obtained by using one or more shielding beads. The beads are most effective when placed on the capacitor leads.

The pulse width will begin to decrease at duty cycles in excess of 25 percent. The circuit in Figure 61 uses a diode to decrease the effect. The maximum period should now be limited to 100μsec.

For periods to 1 millisecond and duty cycles in excess of 95 percent, the circuit of Figure 62 may be used.

By extending the principle, the astable circuit of Figure 63 may be obtained and is useful for frequencies from 20 KHz to 5 MHz. The astable may be gated with the clock input or the J-K inputs.

In the gated mode, the oscillator always will assume the same polarity of output; during the gated off period, the Q output will be low if the J input is the control input and will be high if K is the control input. The resistor values may be mismatched to obtain a pulse generator with duty cycles to about 20 percent. Maximum R_T is 5K.

Lower frequencies (50 Hz to 5 MHz) may be obtained by reversing the polarities of the diodes (Figure 64). When gated as described above, the width of the first pulse will be approximately twice the normal pulse width. Minimum C_T is 50 pf; R_T may be several hundred KΩ.

The oscillator circuit (see Figures 65 and 66) is based on the fact that an odd number of gates in a ring is unstable. The period is adjusted by connecting capacitance to the expander terminal. This oscillator has better temperature stability but poorer waveforms than the previous one. Waveform deterioration limits the lower usable frequencies to 250 KHz.

One-shots also may be obtained from the UTILOGIC NOR gates and OR gates as in Figures 67 and 68. For the circuit of Figure 67, the period is 0.7 $R_T C_T$. R_T must be 8K or less, and C_T 100 pf or greater. The waveform of the $\overline{Y}$ output lacks the sharpness of the outputs of the 320 one-shots shown previously. Maximum period is 5 milliseconds; minimum period is 200 ns.

When only one output is required, the circuit of Figure 68 may be used. The period is 1.1 $R_T C_T$ ±35 percent. R_T includes the input impedance of the OR gate (≈20K). External resistors will reduce the pulse width tolerance to about 15 percent at 2K. The diode will lessen the effect on pulse widths when the duty cycle exceeds 25 percent. When the one-shot requirement is for stable operation and/or wide pulse widths, the SE160 or SE161 should be used.

The NOR gates also are useful as inexpensive, low performance linear amplifiers for certain applications. When used, as in Figure 69, a UTILOGIC NOR gate will have a gain of about 10, and bandwidth of 3 MHz.

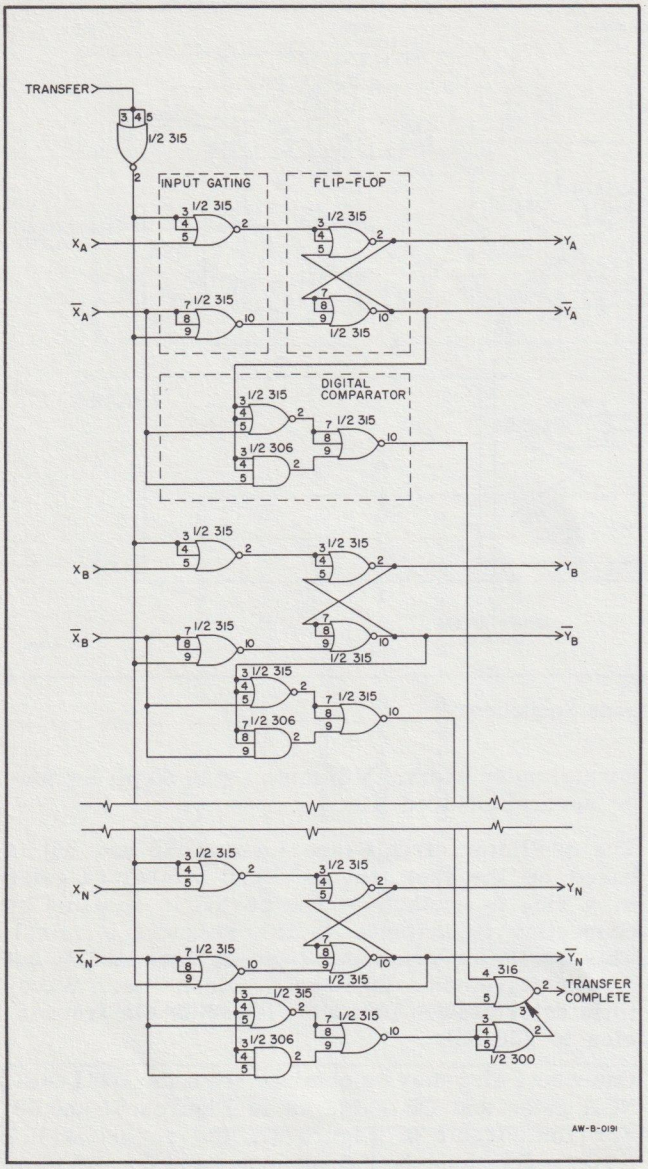


Figure 56 Asynchronous Transfer

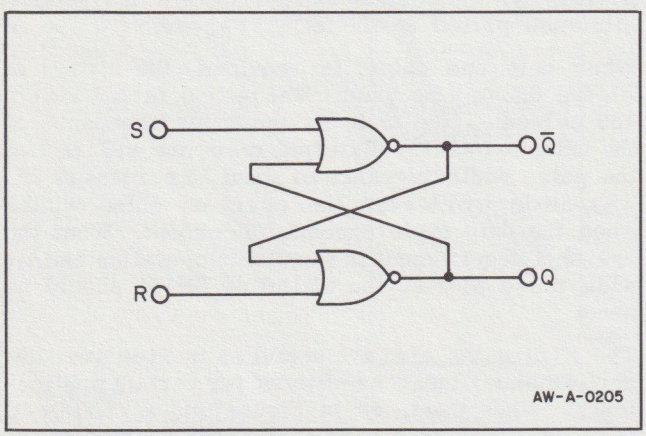


Figure 57 Latch

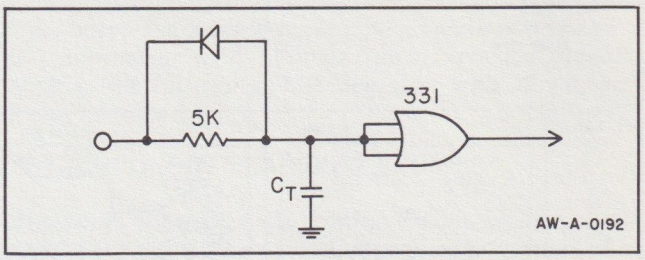


Figure 58 Pulse Width Discriminator

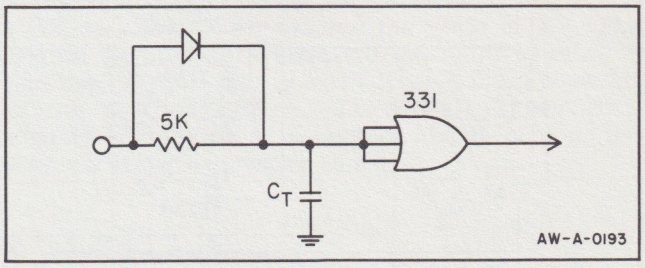


Figure 59 Pulse Stretcher

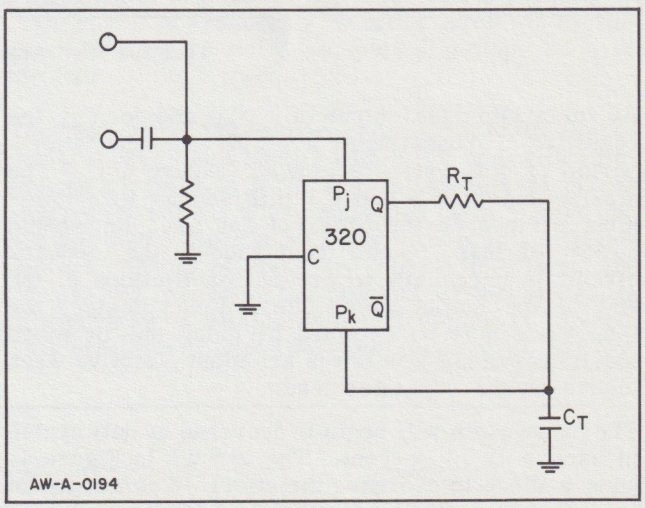


Figure 60 Basic One-Shot

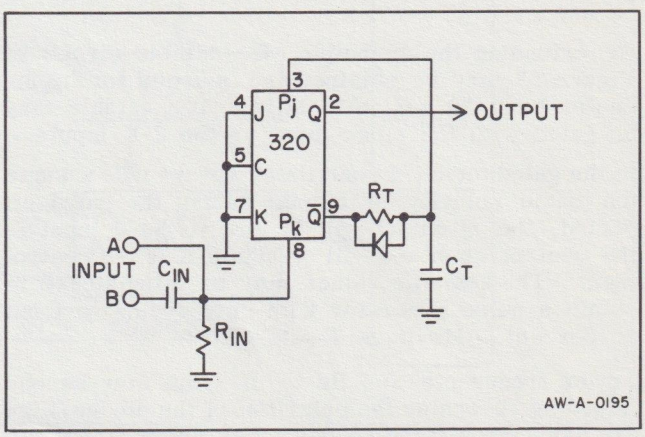


Figure 61 Improved Duty Cycle One-Shot

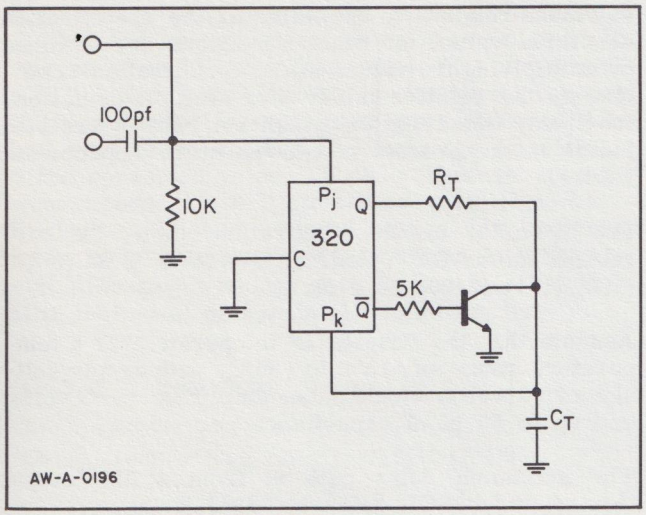


Figure 62 High Duty Cycle One-Shot

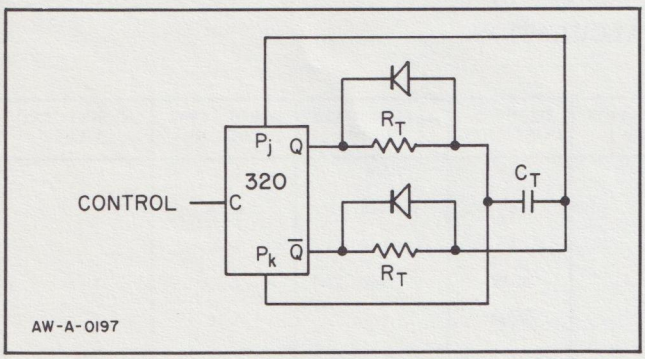


Figure 63 Astable Multivibrator

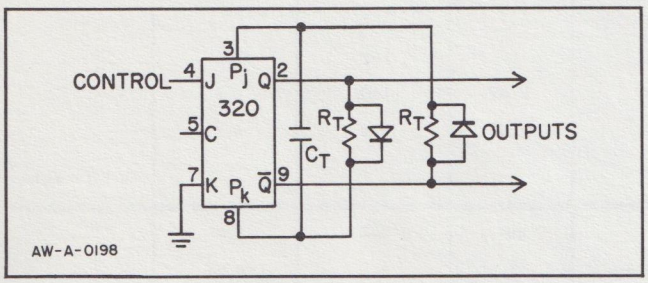


Figure 64 Astable Multivibrator

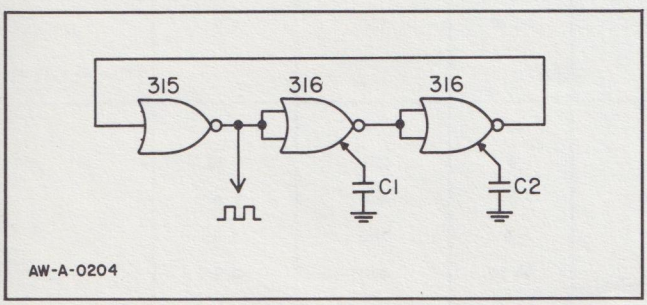


Figure 65 Oscillator

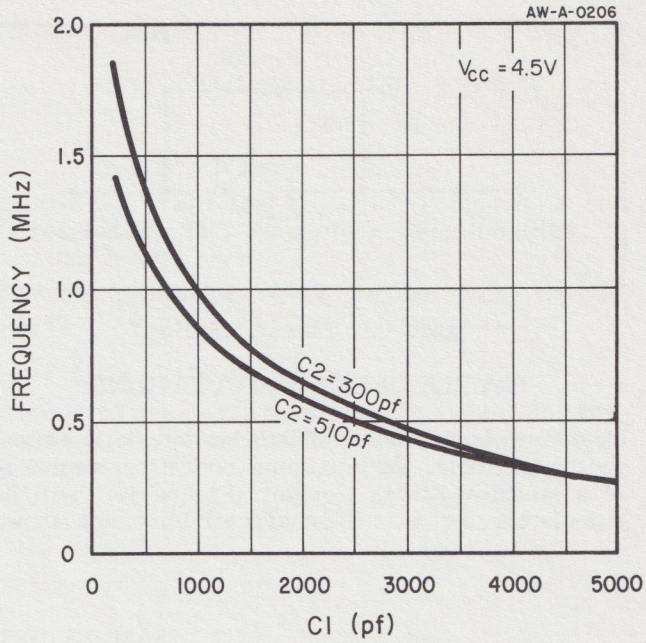


Figure 66 Oscillation Frequency

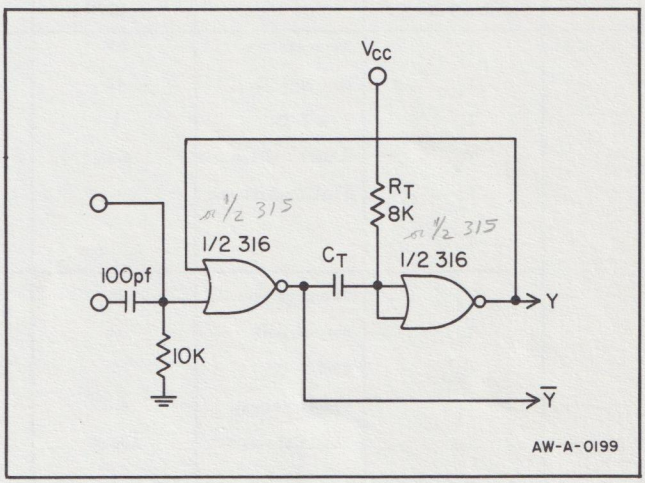


Figure 67 One-Shot with Complementary Outputs

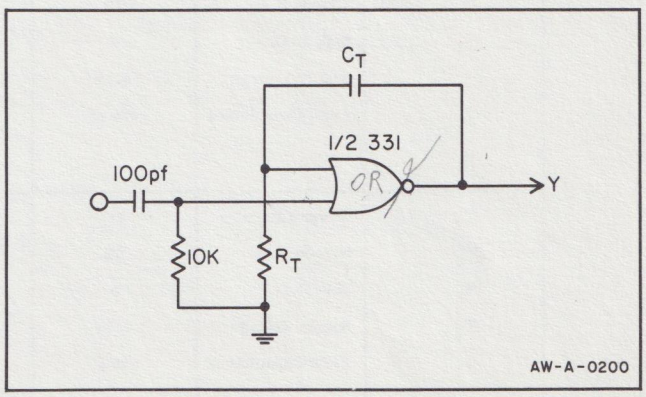


Figure 68 One-Shot

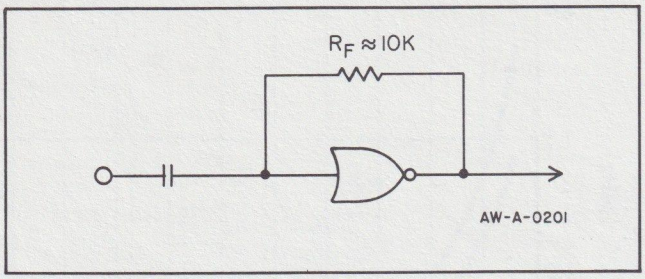


Figure 69 Linear Amplifier

SAMPLE DESIGN CALCULATIONS

To demonstrate the use of the characteristic curves as design tools, the maximum operating frequency of a Modular Binary Counter (Figure 46), will be calculated. Because the characteristics are shown as values relative to the value at the specification condition, values for other conditions are obtained by multiplying the values at the specification condition by the relative value. For multiple deviations from the specification condition, the correction factor is the product of two or more appropriate values.

For example, for the illustration below, the correction factor for T_1 for an SU315 is (1.0) (0.75) (1.0) (1.1) (0.75) or 0.62.

Assume that the counter is to operate over a temperature range of +15°C to +80°C, with supply voltage of +5 volts, clock pulse amplitude of +3 volts, and up to 50 pf of capacitance per output.

The maximum delay path is from a 320 output through three NOR gates to 320 J-K inputs. Two

SAMPLE DESIGN CALCULATIONS

DEVICE	VARIANT CHARACTERISTIC	VARIANT CONDITION	SPECIFICATION CONDITION	SPECIFICATION VALUE (ns)	DESIRED CONDITION	APPROPRIATE CURVE	CORRECTION FACTOR	CORRECTED VALUE
SU315	T_1	Temperature	25°	40	80°	10C	1.0	
	T_1	Source F.O.	12	40	2	10E	0.75	
	T_1	Sink F.O.	5	40	1	10F	1.0	
	T_1	Supply Voltage	4.5V	40	5.0V	10D	1.1	
	T_1	Load Capacitance	130 pf	40	50 pf	10B	0.75	
	T_1							40(0.62) = 25 ns
	T_2	Temperature	25°	70	80°	10C	1.15	
	T_2	Source F.O.	12	70	2	10E	1.05	
	T_2	Sink F.O.	5	70	1	10F	1.0	
	T_2	Supply Voltage	4.5V	70	5.0V	10D	0.9	
	T_2	Load Capacitance	130 pf	70	50 pf	10B	0.8	
	T_2							70(.87) = 61 ns
SU320	T_1	Temperature	25°	80	80°	20B	1.05	
	T_1	Source F.O.	12	80	2	20F	0.95	
	T_1	Sink F.O.	5	80	0	20E	0.9	
	T_1	Supply Voltage	4.5V	80	5.0V	20C	1.0	
	T_1	Load Capacitance	130 pf	80	50 pf	20D	0.9	
	T_1							80(0.81) = 65 ns
	T_2	Temperature	25°	130	80°	20B	1.05	
	T_2	Source F.O.	12	130	2	20F	0.95	
	T_2	Sink F.O.	5	130	0	20E	1.0	
	T_2	Supply Voltage	4.5V	130	5.0V	20C	1.0	
	T_2	Load Capacitance	130 pf	130	50 pf	20D	0.9	
	T_2							130(.94) = 117 ns

calculations will have to be made to determine whether the longest signal delay is associated with changes of the Binary from "1" to "0" or from "0" to "1". The table presents a convenient form on which to record the characteristics and conditions that must be considered and make the calculations to the corrected value. Such a form is strongly recommended since it simplifies calculation verifications. When corrected values for switching times have been computed as shown in the table, total propagation delays may be obtained by summing individual delays in the following way:

For 320 changes from "1" to "0":

$$\text{Delay } (1\rightarrow 0) = T_1(320)+2T_2(315)+T_1(315)$$
$$= 65+2(61)+25 \text{ ns} = 212 \text{ ns}$$

For 320 changes from "0" to "1":

$$\text{Delay } (0\rightarrow 1) = T_2(320)+2T_1(315)+T_2(315)$$
$$= 117 \text{ ns} +2(25) \text{ ns } 61 \text{ ns}$$
$$= 228 \text{ ns}.$$

Figure 20G shows that the clock pulse width required for the 320, for a clock pulse amplitude of 3 volts, is 100 ns.

The total period (T) is obtained by adding the required clock pulse width to the signal delay:

$$T = 228 \text{ ns} + 100 \text{ ns} = 328 \text{ ns}.$$

Therefore, the worst-case maximum operating frequency (f_{max}) of the Modular Binary Counter shown in Figure 46 is:

$$f_{max} = \frac{1}{T} = \frac{1}{328} \cong 3 \text{ Mc}$$

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